

Hardware Design L-Band

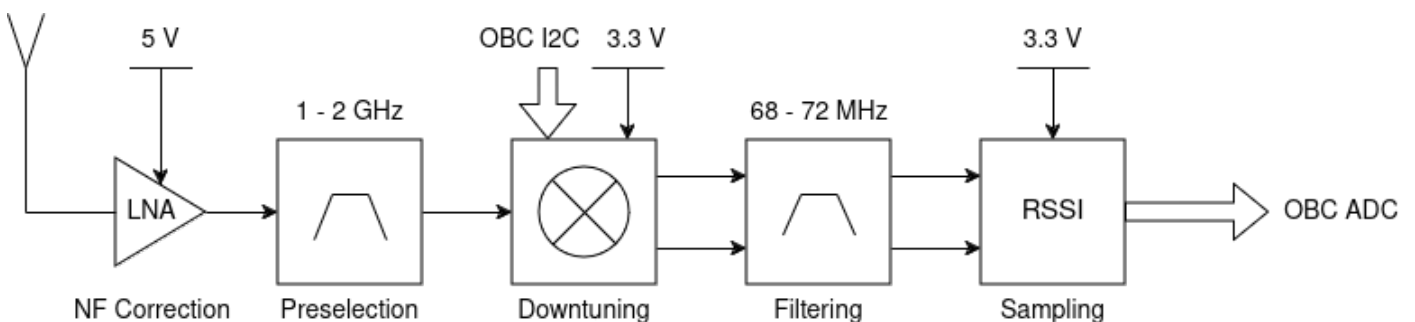
Document scope

This document aims to describe the design process and considerations involved in the designing a L-band Radio Frequency Interference (RFI) payload with the purpose of monitoring and mapping the Electromagnetic Interference (EMI) coming from the Earth in the $1 \leftrightarrow 2$ GHz range in an effort of researching if emergent telecommunication services in this band can be interfering with the GNSS systems and the 1400 $\leftrightarrow$ 1427 MHz band reserved for microwave radiometry. This monitoring receiver consists of 2 main elements: a receiver front-end equipped with a power detector and a deployable antenna.

Front end design

1. Basic architecture

The architecture will be that of a basic, homodyne receiver. The Radio Frequency (RF) input is amplified using a Low Noise Amplifier (LNA), preselected using a cca 1-2 GHz band pass filter and then fed into a controllable frequency tuner, which downconverts the input into near baseband intermediate frequency (IF) for processing. The resulting signal is then filtered using very high Q, low bandpass filter, centred at the desired IF for tune filtering, and passed to a Radio Signal Strength Indicator (RSSI) Integrated Circuit (IC) to sample the spectral element's power and direct the data to the On Board Computer's (OBC) Analog to Digital Converter (ADC) input.



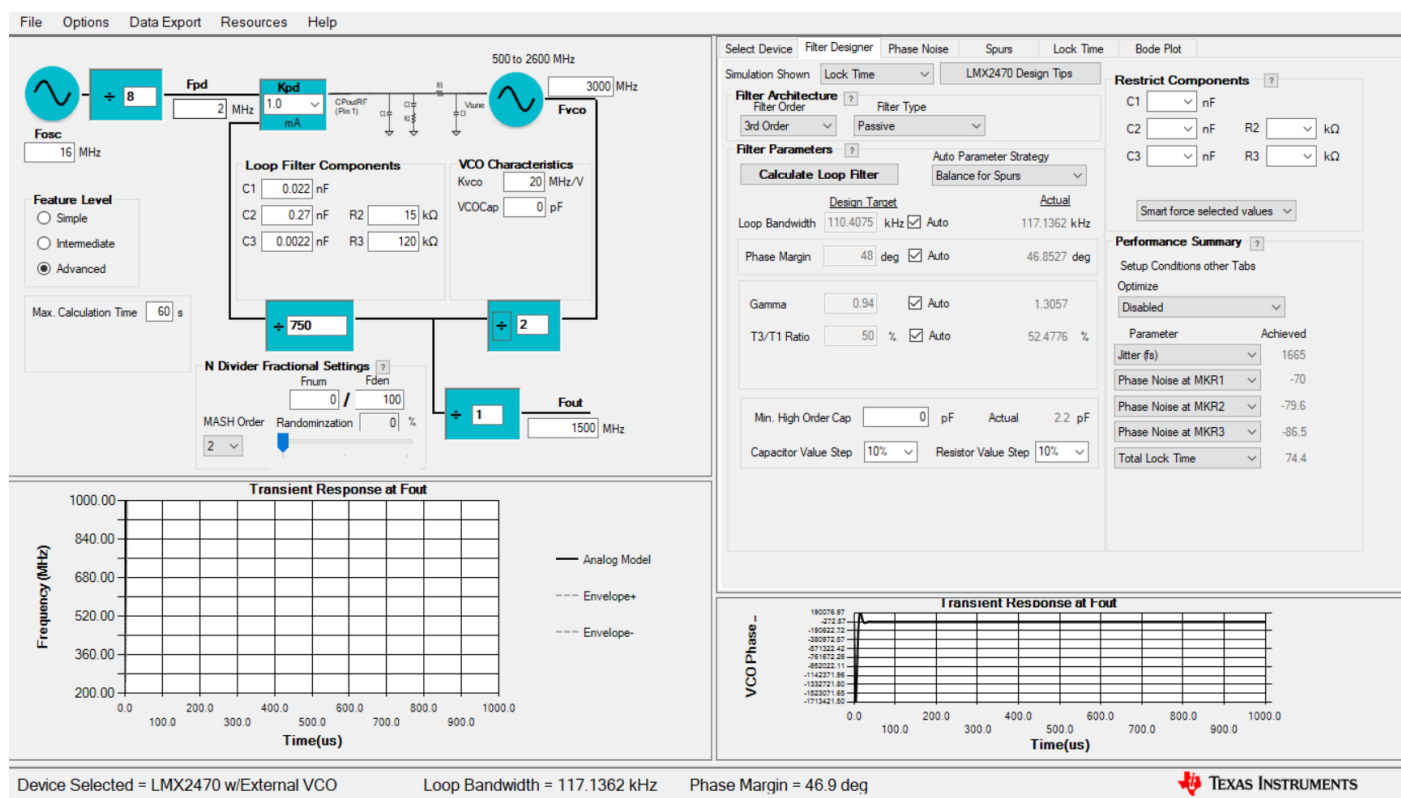
2. Functional schematic and IC choice

In order to translate the abstract choice of architecture into a functional schematic, components are required that fit the rather strict requirements explained previously. With the ongoing global semiconductor shortage, and the small satellite industry increasing its dependency on Components Off The Shelf (COTS), the design choices from this point onwards have been heavily influenced by the distributors' availability and stock.

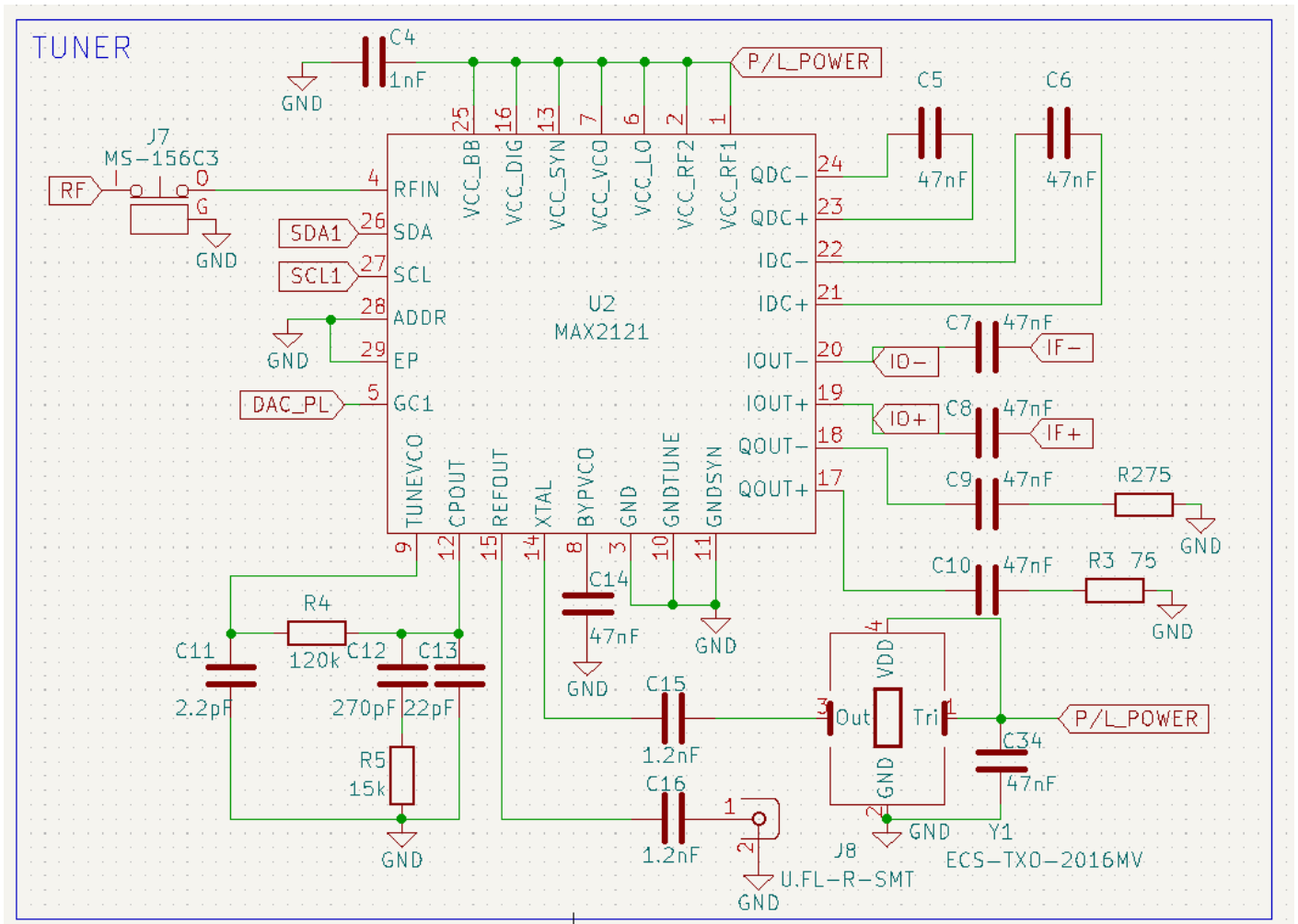
To kick off, the most restrictive element, in terms of the aforementioned limited availability, will be discussed: the downconversion tuner. It is worth mentioning that initial designs envisioned a simple passive mixer with a standard Local Oscillator (LO) in the form of a wideband Voltage Controlled Oscillator (VCO) controlled by the OBC's Digital to Analog Converter (DAC) output. However, due to image frequency issues inherent to such superheterodyne architectures, as well as the continuous dwindle of adequate VCO and IF filter pairs, this simplistic design has been forcefully discarded. The current iteration is therefore based on **MAX2121** direct-conversion L-Band Tuner IC originally used for Television through Satellite (TVSAT) applications. The chip sports 24 I2C controllable monolithic VCOs, a complete fractional-N Phase Locked Loop (PLL) circuit covering the 925 ↔ 2175 MHz frequency range, internally adjustable amplifiers offering up to 80 dB of gain, active mixers which eliminate the image frequency issues, double differential output for both I and Q modulation elements, and integrated 123 MHz IF output low pass filters, all on a minute 5 mm X 5 mm, 28 pin TQFN package. In terms of disadvantages, one could point out the high power consumption of cca 150 mA at 3.3 V line voltage, a 75 Ω matched input and output lines, as well as a staggering Noise Figure (NF) between 8 and 12 dB, depending on the amount of adjustable gain desired. While these weak points are all valid sources of concern and are addressed in the following component descriptions, a mention should go to the termination impedance. As the chip has been designed for TVSAT applications that have since seen less and less usage, the 75 Ω specific impedance is introducing issues in finding matched LNAs and Filters in the COTS market, with the few options still existing either not being wideband enough, having too high a consumption or centered in other frequency bands, as most of the industry has moved to 50 Ω terminations, resulting in opting for components of the latter impedance with the possibility of introducing a matching network. As the reader can already begin to observe, the design choices are intricate and bidirectional, with cascading changes affecting all component choices.

In terms of biasing, the **MAX2121**'s integrated N-fractional PLL most notably requires a reference frequency provided by means of a discrete crystal oscillator, with the value being chosen as a tradeoff between on one side the maximum Equivalent Series Resistance (ESR) and spectral resolution obtained at the front end output to a commonly-found value of 16 MHz. Additionally, while the feedback divider in the form of the Synthesizer block is itself incorporated within the chip, for achieving control, an external control loop is required between the output of the charge pump (CPOUT) and the VCO tuning (TUNEVCO) pins. The 3rd order filter configuration shown below has been obtained as a result of a software-assisted analysis using *Texas Instruments' PLLatinumSIM*

simulation tool, optimising for stability and locking time of less than 50 us, allowing for a sweeping step of 2 MHz, when operating the tuner by writing in the N-Divider, F-Divider, R-Divider registers 1,2,3,4,6 and 7 of the chip's internal memory bank.



Lastly, an array of filtering and DC-blocking capacitors have been added to multiple pins as per the manufacturer's instructions.

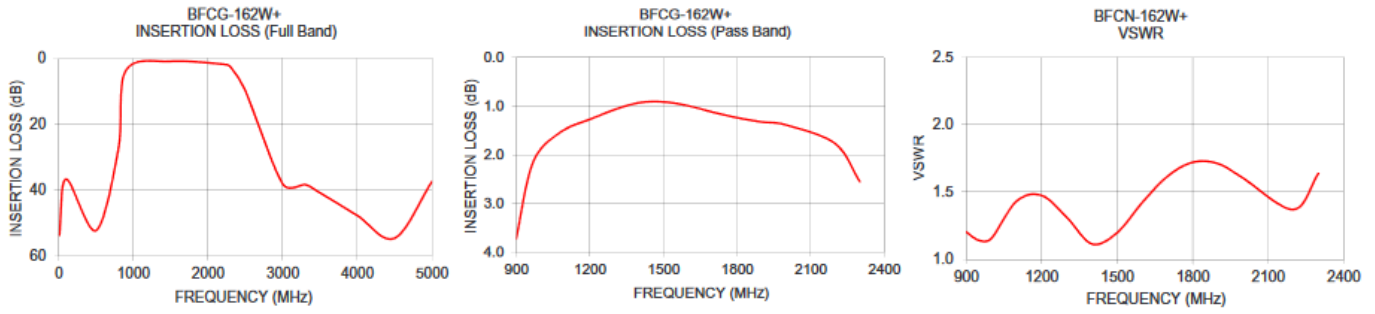


Before continuing, it is worth discussing the previously mentioned possibility of introducing an adaptation network at the input of the tuner to convert the $50\ \Omega$ of the preceding elements to the $75\ \Omega$ of the MAX2121. Considering both that the RF chain covers a very wide band (from 1 to 2 GHz), and the PocketQube's strict power and space limitations, the solution considered was a L-pad resistive network made with two broadband SMD resistors of 43 and 91 Ω respectively, trading approximately 5.6 dB loss for the simplicity and broadband nature.

On the other hand, in the event in which the choice is made not to implement this adaptation network, considering the signal level at the input of the tuner being cca -86 dBm, a transition from the $50\ \Omega$ to $75\ \Omega$ specific impedance will imply a reflection coefficient of 7 dB, which, considering also the band pass filter insertion loss of 3 dB and the LNA's isolation of 22.5 dB, will translate into a *back-radiated signal at the antenna of cca -118.5 dBm*, significantly lower than the computed noise floor of -105 dBm, with no chance of harming the intermediate components. In light of this, the choice of adding said adaptation network has been discarded.

Moving back the RF chain, the preselection filter has been chosen in the form of the $950 \leftrightarrow 2200$ MHz **BF CG-162W+** ceramic bandpass filter. Its desirability originates from its extremely wide passband, minute size (2 x 1.25 mm equivalent to 0805 imperial casing), LTCC construction and very good stability with temperature, combined with $-55\text{C} \leftrightarrow 125\text{C}$ operating range. One downside could be the fact that its band doesn't perfectly match the $1 \leftrightarrow 2$ GHz RF input specified by the requirements. This is not a critical aspect however, as the final reading can be controlled from the OBC sweep, and the extra tail-ends are not significant. Moreover, the stop band insertion loss of

upwards of 40 dBs ensures no undesired spectral elements outside of the band would interfere with the payload input, at the cost of cca 3 dB of pass band insertion losses.



Next up, while the gain of the previously presented tuner is itself more than enough to bring any incoming signal from the noise floor of cca -105 dBm (please refer to the IF filter description below) to the -77 ↔ 9 dBm sensitivity range of the RSSI (please check the Gain Budget section below), the tuner's noise figure of 8 dB (at minimum gain) will decrease the performance of the receiver substantially. To this end, the **LEE2-6+** LNA has been placed at the start of the RF chain to provide a 21-19 dB preamplification along the whole L-band, with a very low power consumption of 16 mA at 5 V. This way, this chip's better NF of 2.3 dB (at 2 GHz), when placed before the tuner, will, alongside with the insertion loss of the Preselection Filter that follows, heavily improve the receiver's overall NF:

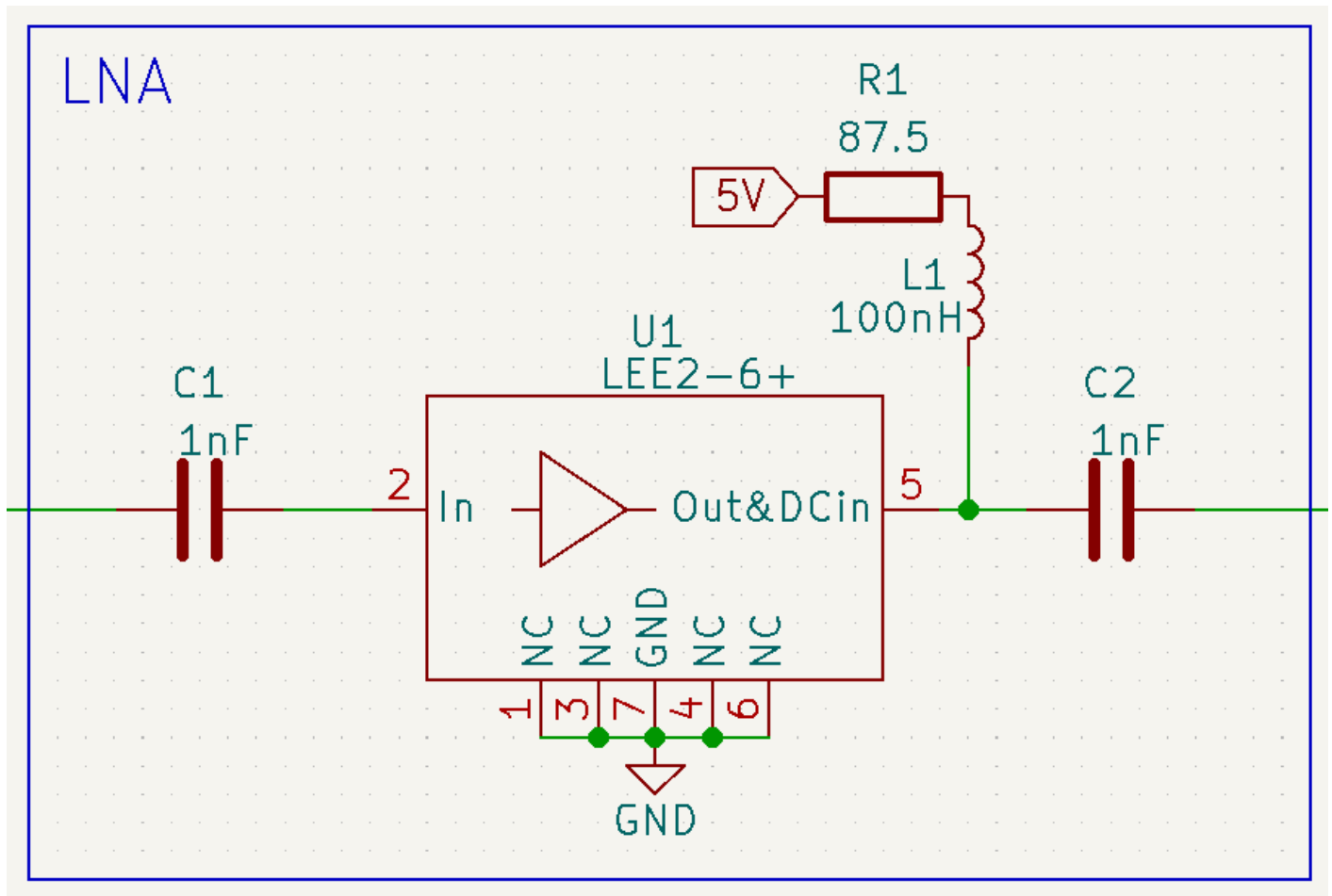
$$NF_{Total} = NF_{LNA} + \frac{G_{Filter} - 1}{G_{LNA}} + \frac{NF_{Tuner} - 1}{G_{LNA} * G_{Filter}}$$

$$NF_{Total} = 10^{\frac{2.3}{10}} + \frac{10^{\frac{3}{10}} - 1}{10^{\frac{19}{10}}} + \frac{10^{\frac{8}{10}} - 1}{10^{\frac{19}{10}} * 10^{\frac{-3}{10}}}$$

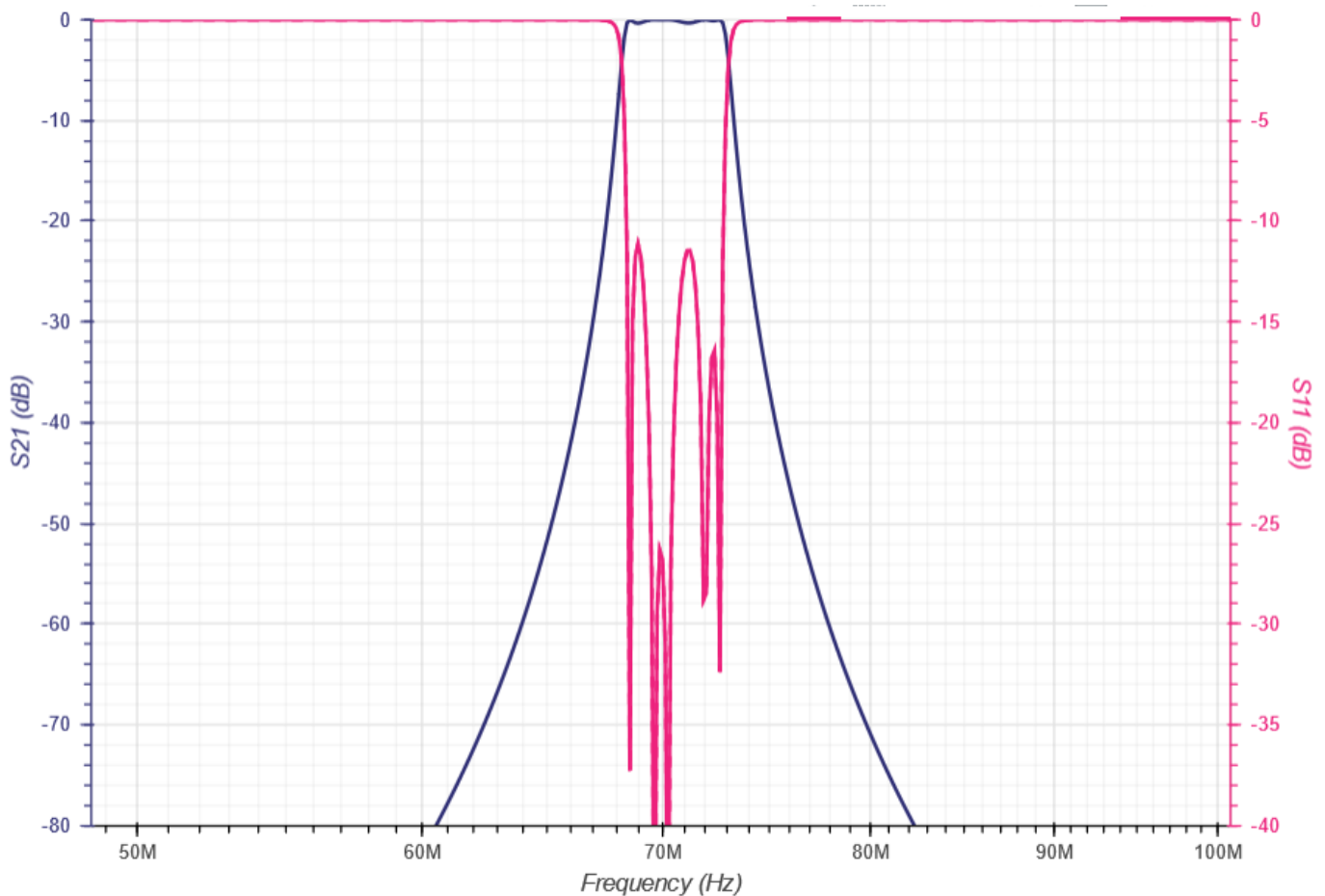
$$NF_{Total} = 1.7 + \frac{0.5 - 1}{80} + \frac{6.3 - 1}{80 * 0.5} = 1.82 = 2.61dB$$

In terms of circuit biasing, the IC is attacked in current, with nominal operation being obtained when supplied 16 mA at 3.6 V. To this end, a SMD resistor has been chosen to bridge the 1.4 V drop as a current source of the required amperage, resulting by Ohm's law in a 87.5 Ω value. The only other required components are two DC-block capacitors for both the input and output of the

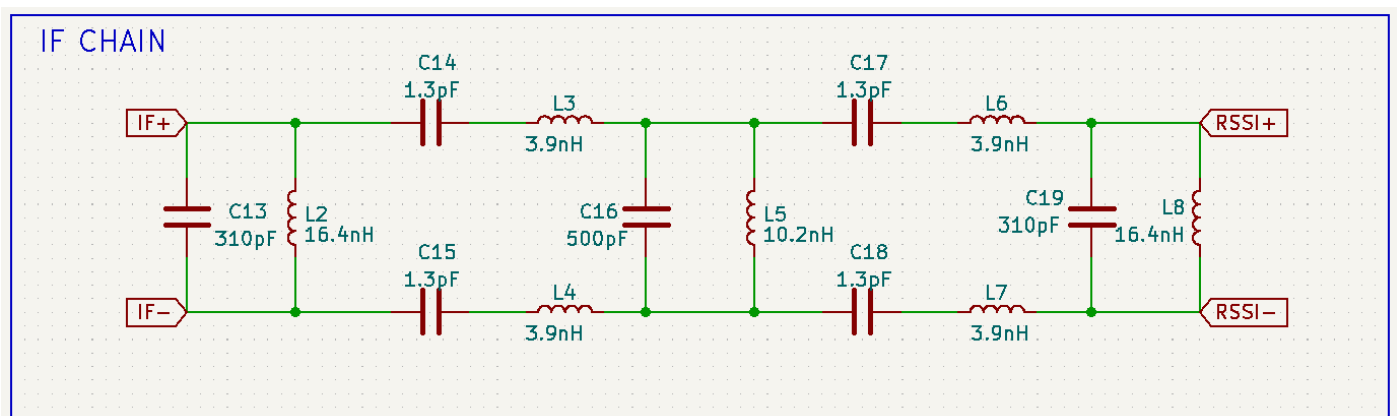
IC, as well as a RF choke for the supply. The values of these components are frequency dependant and are computed for each chain: for the inductors, their self resonant frequency must be considerably higher than the working frequency: 100 nH and 3.3 uH for the RF, while the capacitors being chosen so their cutoff (-3dB) frequency lower than the working frequency: 10 nF for the former link, and 1 nF for the latter.



Furthermore, following the tuner, the 5'th order shunt first Chebyshev band pass filter centered at 70 MHz shown below has been implemented, sporting a 4 MHz narrow bandwidth, negligible insertion loss and 0.1 dB passband ripple. The choice of the central frequency has been made as result of filter optimisation, upper limit of the tuner's integrated Low Pass Filters (LPF), combined with distancing from the very low frequencies in order to avoid coupling with any Pulse Width Modulation (PWM) elements introduced with voltage boosters and other switching regulators used within the satellite.

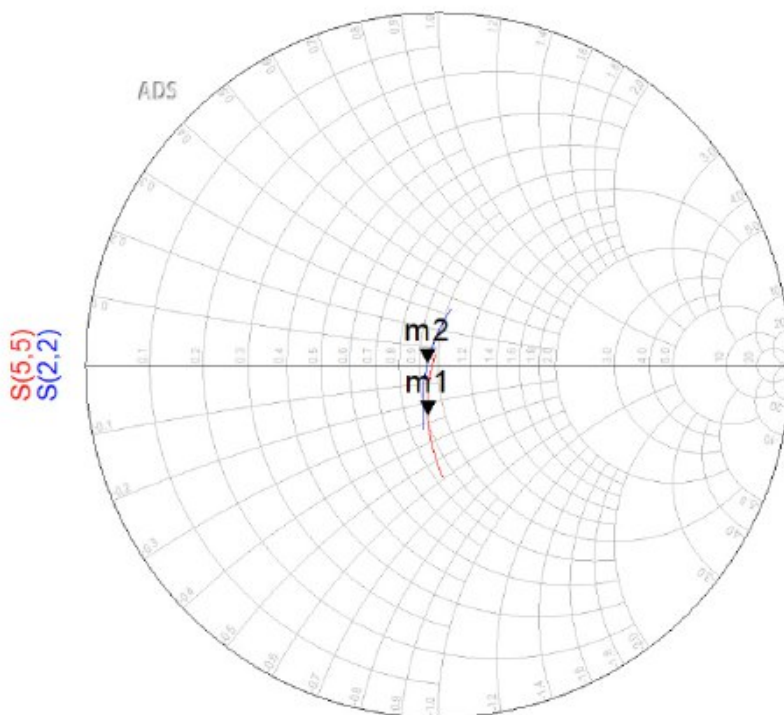
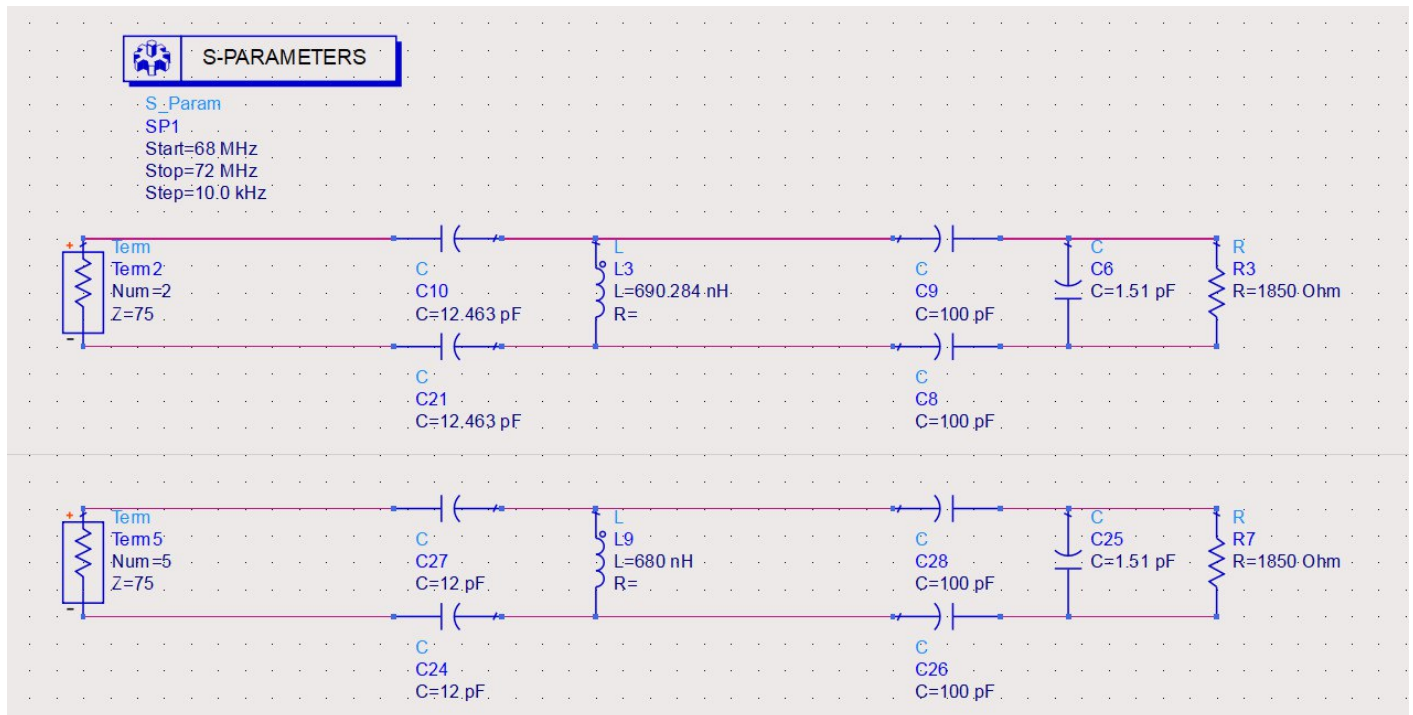


The purpose of this added filter is to provide a good element isolation with its narrow band and high isolation, resulting in an system spectral resolution of 4 MHz, after the sampling. Additionally, as both the tuner output and RSSI input are differential, the filter has been implemented likewise, complete with 75 Ω matching complying with the **MAX2121** integrated terminations. Thus, the IF chain enjoys reduced electromagnetic interference (EMI) production, reduced sensitivity to induced or coupled noise, less distortion of edges due to signal reflections.



Next up, The RSSI detector upon which the payload is based is Linear Technology Corporation's **LT5537** chip. This chip provides a log-linear output response that depends on the RF power at its input and is able to measure RF power from 10 MHz to 1000 MHz, with the input being set by the previous filter to 70 MHz. At this frequency, the RSSI detector has a single ended sensitivity of -77 dBm with the advantage that, by using the high impedance differential input adapted using a

matching network from the 75 Ω characteristic impedance of the the previous elements to the 1.85 k Ω & 1.51 pF equivalent parallel RC of the RSSI as per the manufacturer's specifications, the sensitivity can be further improved to values as low as -82 dBm at the working frequency. The matching network is a simple LC configuration and has been obtained using the Keysight Advanced Design Software (ADS), with the results displayed below corresponding to their theoretical and real market component values:



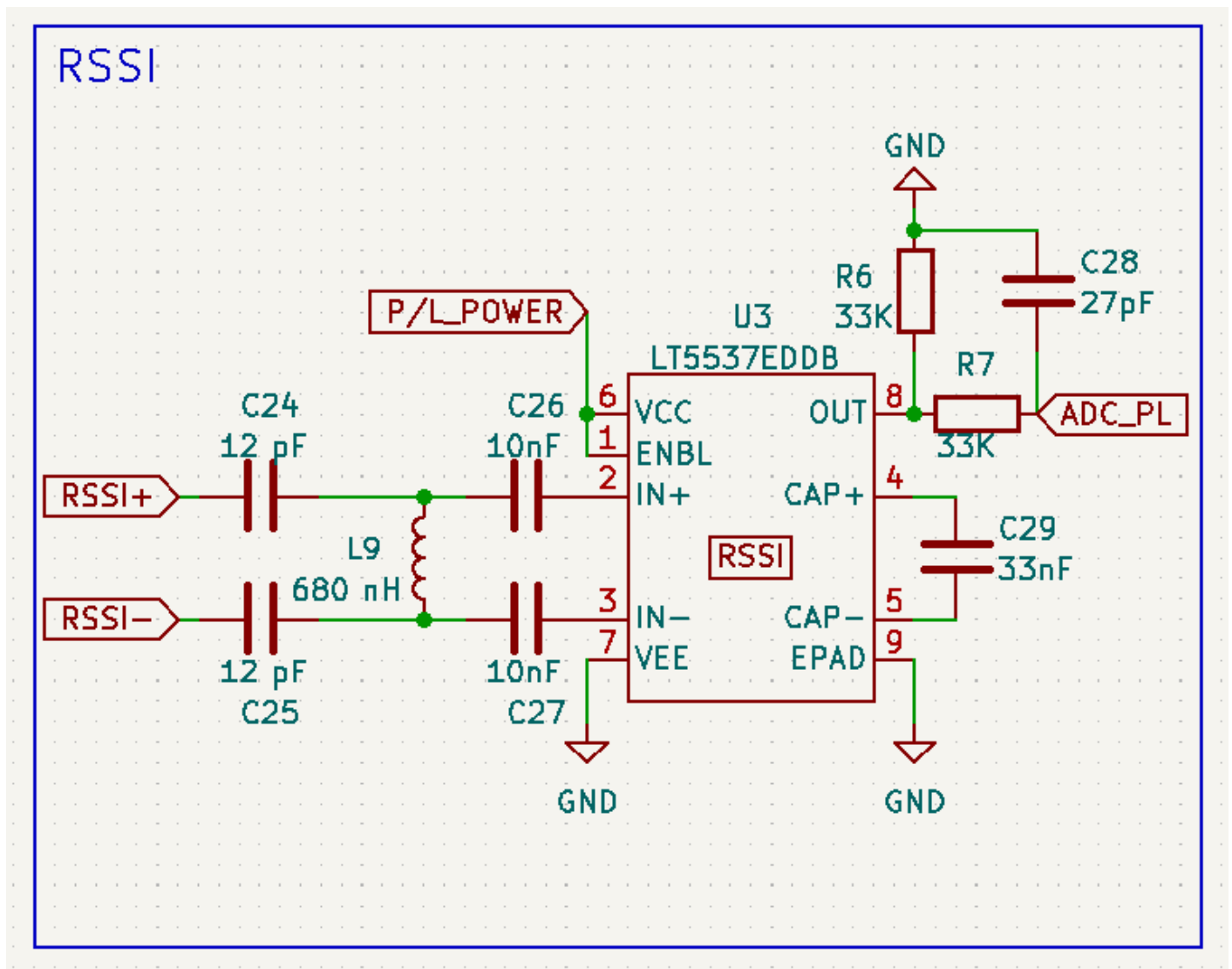
m2
freq=70.00 MHz
 $S(2,2)=0.031 / 170.250$
impedance = $Z_0 * (0.941 + j0.010)$

m1
freq=70.00 MHz
 $S(5,5)=0.144 / -101.613$
impedance = $Z_0 * (0.908 - j0.262)$

freq (68.00 MHz to 72.00 MHz)

Additionally, by using DC blocking capacitors at the input, along with a 33 uF capacitor in the external feedback loop, a phase margin of 84 degrees has been achieved, resulting in increased stability, with the load resistor of 33 kΩ providing an output log-linear rate of 20 mV/dB. Lastly, a simple low pass filter has been added at the output to allow the ADC sampling frequency to comply with the Nyquist limit. What this means is that, due to the ADC's limitation of maximum sampling frequency, the signal it receives needs to be limited to a maximum bandwidth that the LPF limits. This however introduces the issue that, while fully capable to detect slowly changing input power, some high spectral elements (sudden changes in time) will not be detected, with this problem being accepted as a design limitation. Considering the most permissive and restrictive of sampling rates of the STM32L476:

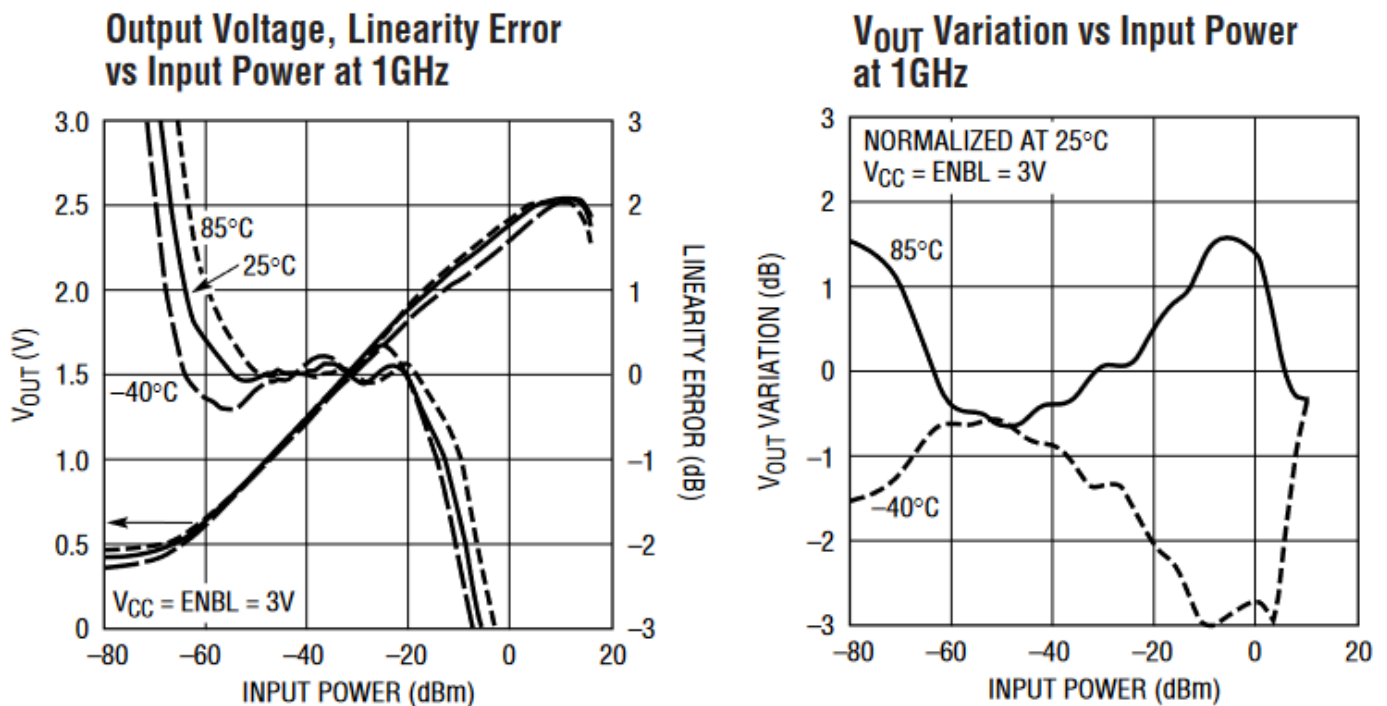
The fully biased configuration is thus showed below:



In what follows, the gain budget will be analysed.

Component	Name	Gain [dB]
Low Noise Amplifier	LEE2-6+	19
Bandpass filter	BFCG-162W+	-3
Homodyne Tuner	MAX2121	78
Chebyshev filter	N/A	-0.5
TOTAL GAIN		93.5

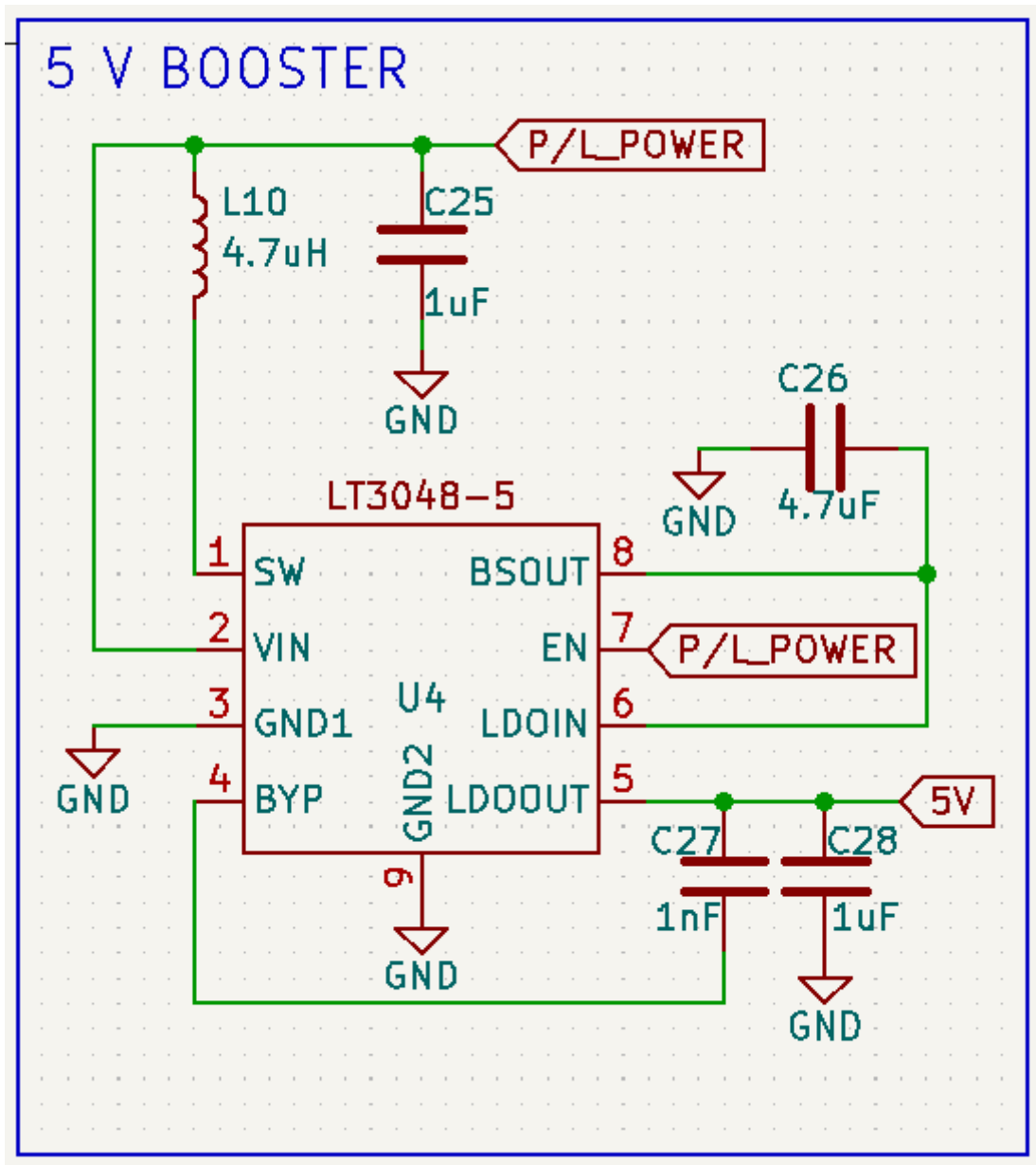
Considering an overall receiver bandwidth of 4 MHz (as given by the most restrictive filter), a ground noise temperature of 290 K and the equivalent Noise Figure obtained previously in the LNA section of 2.61 dB, one can obtain the background noise level of -105 dBm at the antenna input. As a result of this, along with the total front end gain, the RSSI input power can be obtained as being approximatively -11.5 dBm, falling well into its sensitivity range. By correlating this level with the Input Power - Output Voltage characteristics provided by the manufacturer, the reader can notice that the front end chain amplification is more than sufficient to allow low power signal acquisition. On the other hand, the maximum input power the RSSI can register is 9 dBm, allowing for reception of high power signals up to -84.5 dBm (sensed at the antenna output), resulting in a dynamic range of 20.5 dBs. In the light of this, one argument could be made that, if one was to proceed with the inclusion of the 50 Ω to 75 Ω matching network and thus decreasing the FE gain, the overall receiver dynamic range would be increased to 29.5 dB. At this stage of the design process, it has been decided that such a gain would not be worth it.



Moreover, within the -60 $\leftrightarrow$ 10 dBm range of Input Power, provided it is used at positive temperatures, the RSSI Output Voltage graph follows a cvasi-linear figure, which is empirically

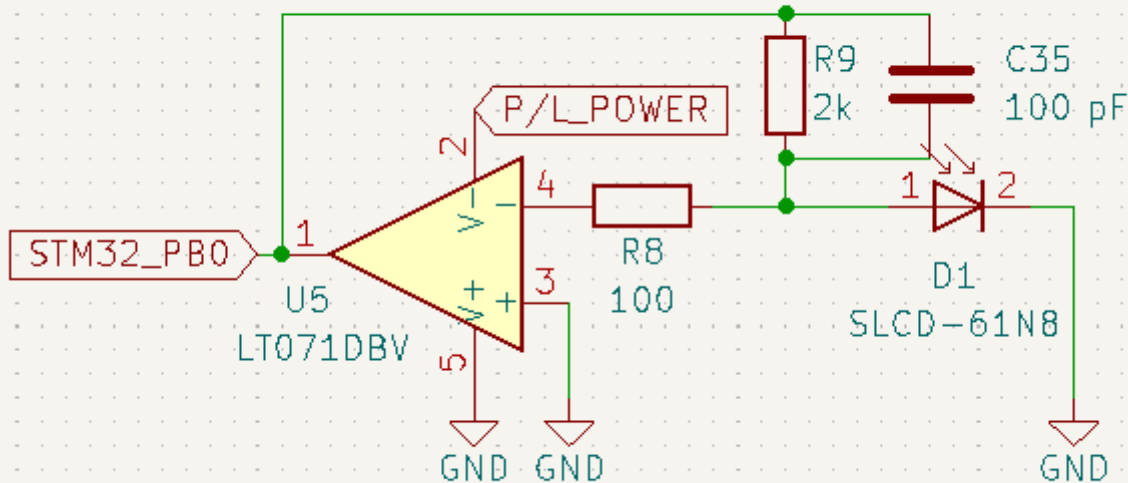
deduced in the ³Cat-NXT Integration and testing book, under the appropriate *Functional tests* page.

Additionally, in order to supply the LNAs, a 5V boost converter in the form of **LT3048-5** has been used, with the biasing elements respecting the manufacturer's specifications.

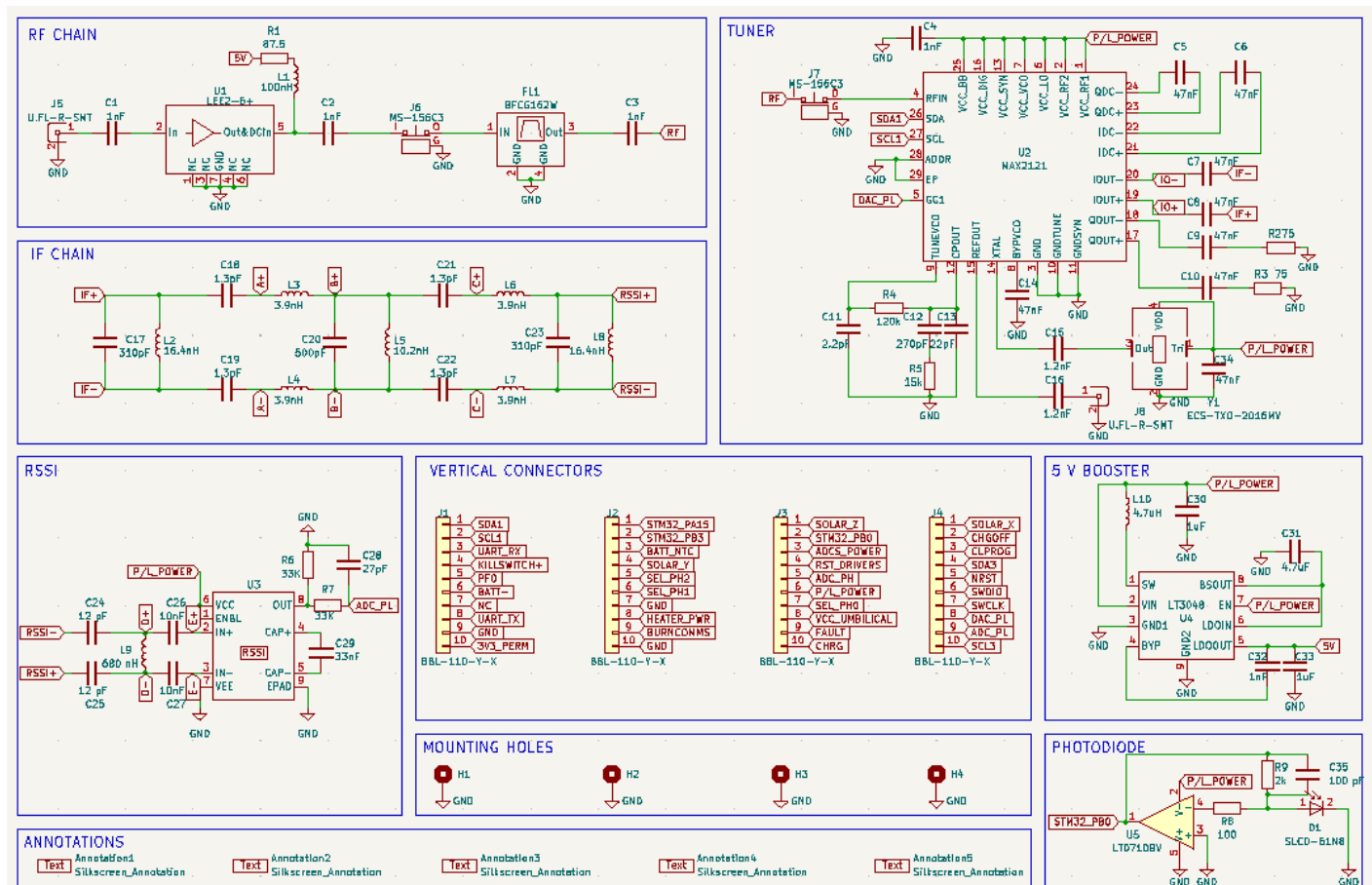


Finally, as the current design iteration envisions a stowable broadband helical antenna (more on that on the appropriate section below), after its deployment, the payload board will be the de-facto top board of the PocketQube. In accordance with the requirements regarding the Sensor Module of the Attitude Determination and Control System (ADCS), and more specifically with the need of photodiodes on all sides of the cube, one such device has been installed on this payload's board upper face in the form of **SLCD-61N8**. However, as this photodiode's output signal is very small (cca 170 uA) and its connection does not follow the usual path through the Breakout Board, where a series of Operational Amplifiers (Opamps) have been used to amplify this signal to bring it within the sensibility of the OBC's ADC, one such device was employed, in the form of **LT071DBV**, biased in order to match the amplification factor of the other Opamps in order to avoid sensor data misscalibration, with the resulting signal being routed through the multifunctional **STM_PBO** pin.

PHOTODIODE

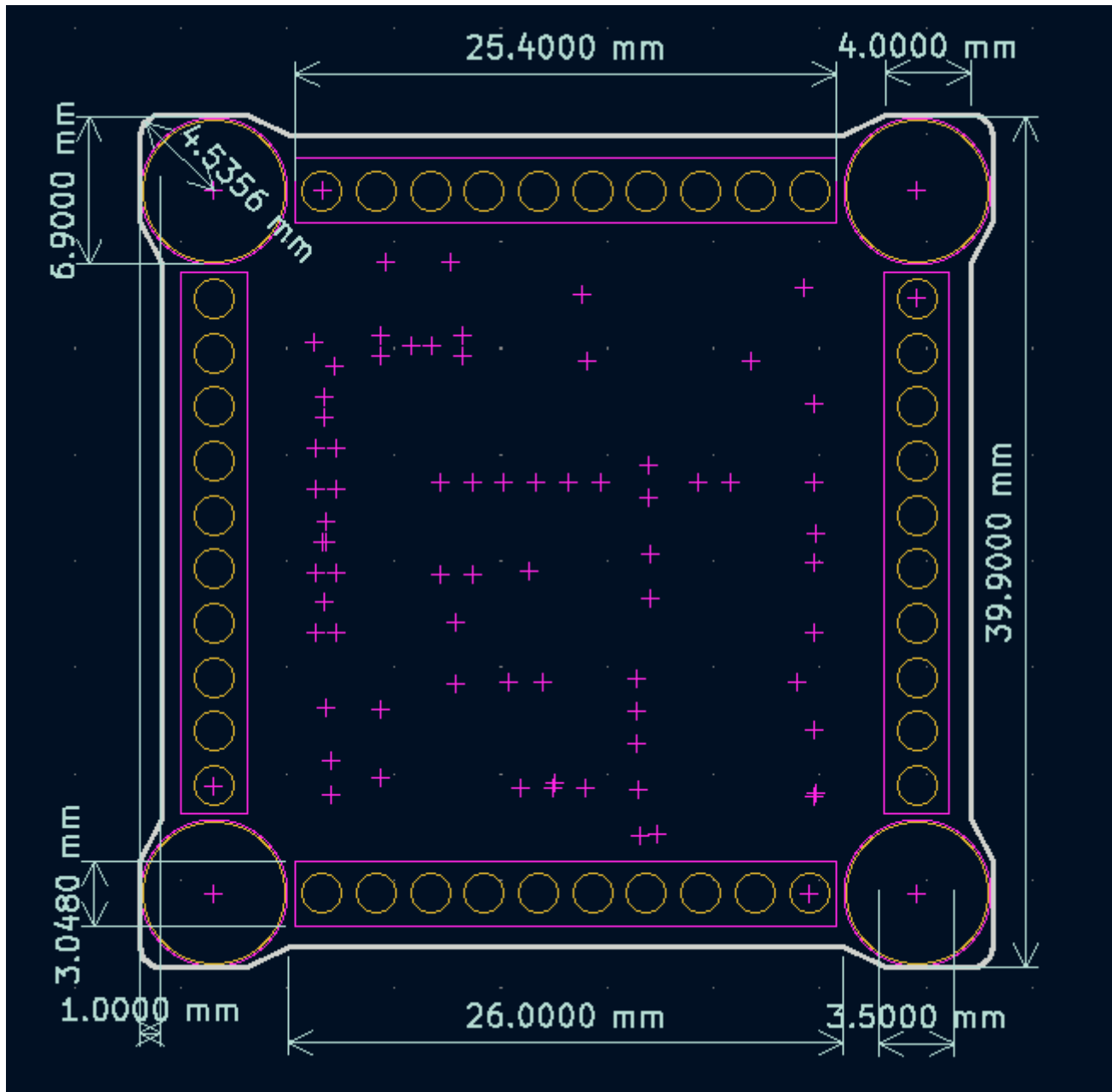


To conclude this section, the complete schematic can be consulted below:



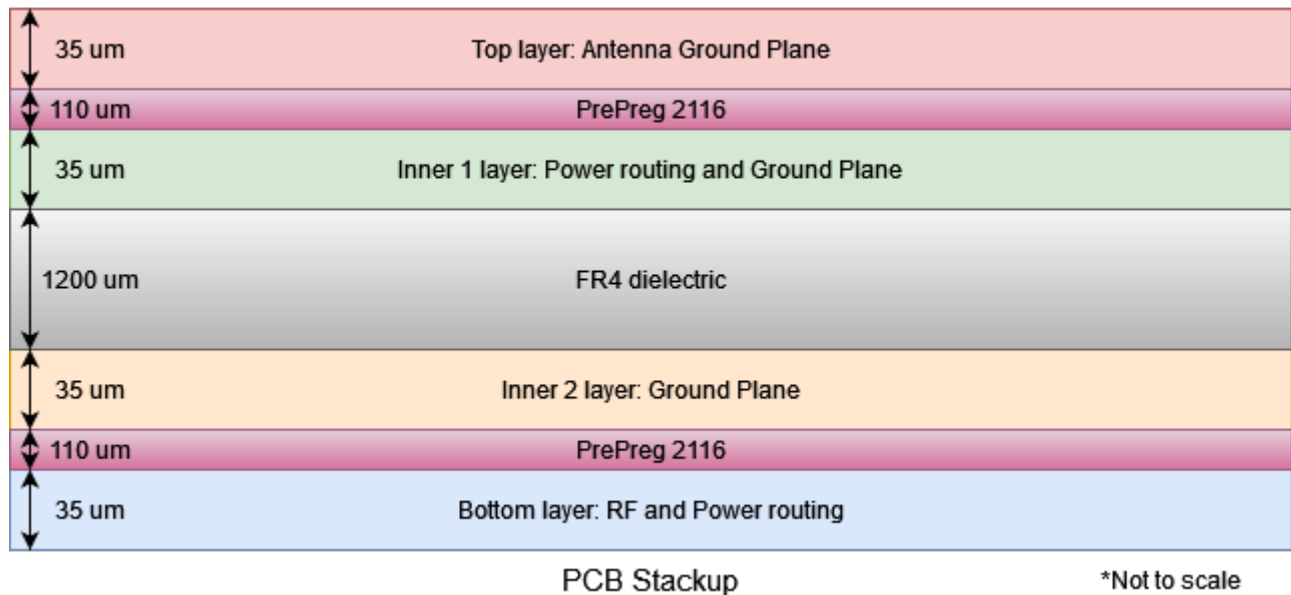
3. Printed circuit board design

To begin, as this Payload's Printed Circuit Board (PCB) will be part of the PocketQube's central PCB stack, it needs to comply with said standard, presented below, having fixed the outline, dimensions and locations of both the 4 screws and vertical connectors. In terms of connectors, the **SLW-110-01** has been replaced with the far slimmer **BBL-110** as there is not other upper PCB to be connected, and only the inferior set of pins are needed to complete the vertical connection to the OBC&COMMS board beneath.



Next up, a big design factor consists in the helical antenna high space occupancy (current design iteration involves a 34 mm diameter coil being stowed and deployed from above the PCB) which resulted in the decision being made to place the entirety of the front end elements on the bottom layer, with the exception of the photodiode because of reasons explained previously as well as the **C.FL-R-SMT-1** coaxial connector, with the resulting blank top layer acting as a 40 x 40 mm ground plane for the antenna. Additionally, as this board will be exposed to sunlight after the antenna deployment, in accordance with the thermal analysis, the soldermask color has been set to white. Furthermore, as the Coplanar Waveguides have been used for the RF Transmission Lines (TL), and

they require by definition a ground plane underneath the trace, another of the former has been added just above the bottom layer (as seen from the nominal PQ positioning), thus creating the need for inner layers. Moreover, as the number of fabricable inner layers tends to be imposed by manufacturers to be even, an additional layer has been employed between the top layer and the ground plane layer for the bottom layer, which has been used for power lines and analog small signal routing. The final stack-up can be seen below.



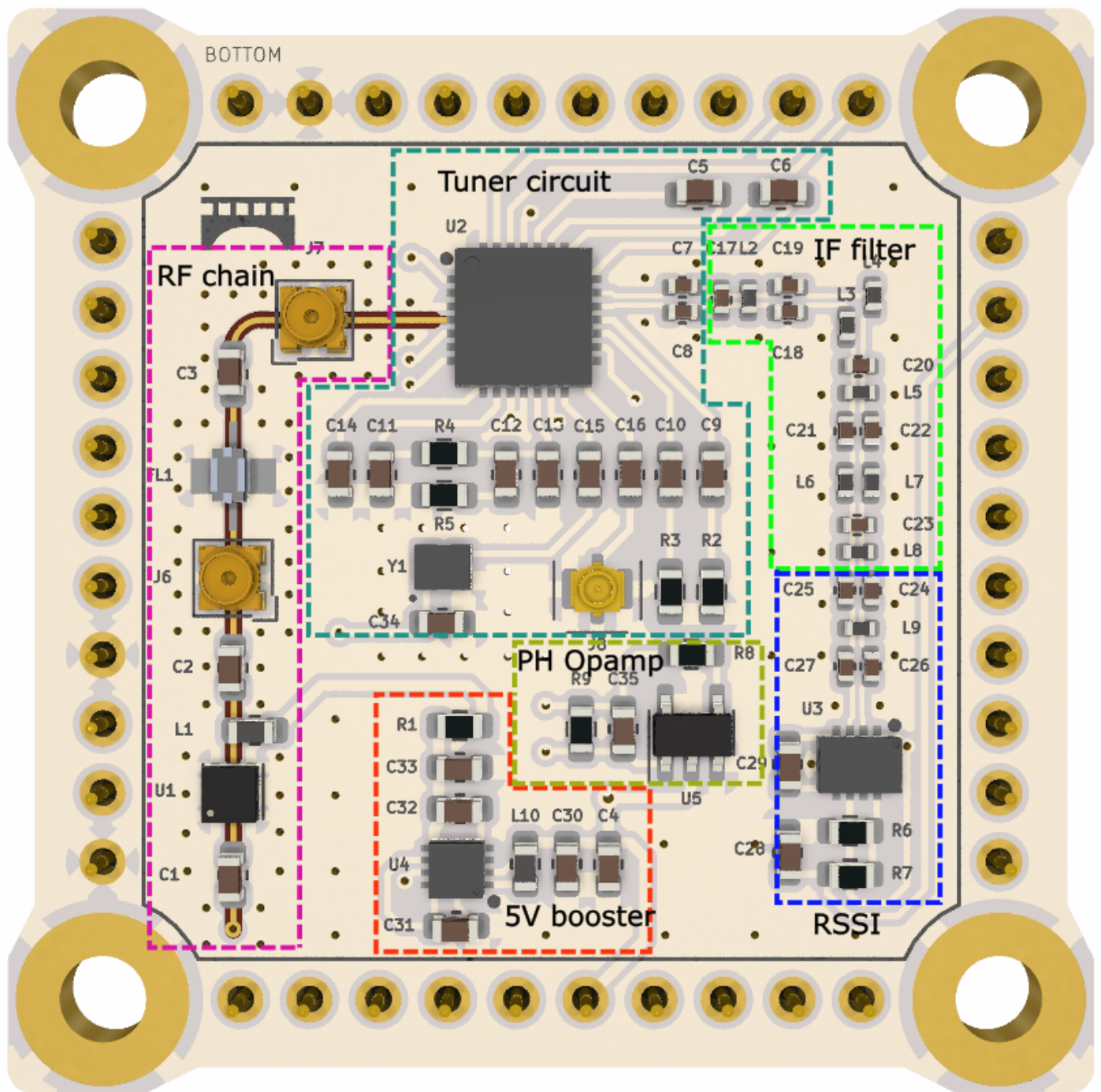
Before diving into the bottom layer implementation, a study has been performed both using KiCad's integrated calculator, as well as Saturn PCB Design Toolkit in order to obtain the required dimensions for traces and vias corresponding to the characteristic impedances of 50 Ω for the RF chain and 75 Ω for the RF chain respectively, with the results being shown in the table below. Additionally, the detailed simultaion snippets are attached to this page.

Design Rule Routing

Impedance	Track width	Track clearance	Via hole diameter	Via pad diameter	Via plating thickness	Differential width	Differential spacing
50 Ohm	0.21	0.22	0.3	0.6	0.035	0.32	0.2
75 Ohm	0.1	0.22	0.3	0.6	0.035	0.185	0.15

*All dimensions are in mm
 *All unspecified specs are PCBways minimum requirement specs.

Starting with the **RF chain**, as can be seen in the left part of the broken down picture of the board below, it presents a standard TL structure, with components being placed in a straight line, surrounded by a RF via fencing, and with the solder mask removed, in order to reduce losses and preserve the characteristic impedance. Also, as the chain is comparable to the length of the PCB, it has been reoriented using a circular 90 degrees bend to minimise reflections.



Now would be an adequate time to raise the reader's attention to the **MS-156C3** Hirose probe headers (J6 and J7) present both before the bandpass filter and before the tuner. They consist of an internally matched 50 Ω coaxial termination, fit for same family SMA conversion adapters, allowing for easy on-board testing of the TL. Worth mentioning is that, when introducing the probe in the header, a mechanical switch is activated, the input of the switch being connected to the probe input, *while disconnecting the output of the header*, thus rendering the effect of the rest of the front end moot. This way of operation allows for one way testing, thus reducing the number of effects that can affect a measurement and isolating possible error factors.

Next up, the **MAX2121** tuner's biasing has been done by having the filtering and DC-blocking capacitors, as well as the Loop filter and crystal oscillator as close as possible to their respective pins while not affecting the TLs. Noteworthy in this part is that the crystal oscillator working at 16

MHz has been placed within a via guard ring in order to minimise cross-talk, and the addition of a **C.FL-R-SMT-1** coaxial header connected which allows access to the tuner's inner synthesising frequency for testing purposes.

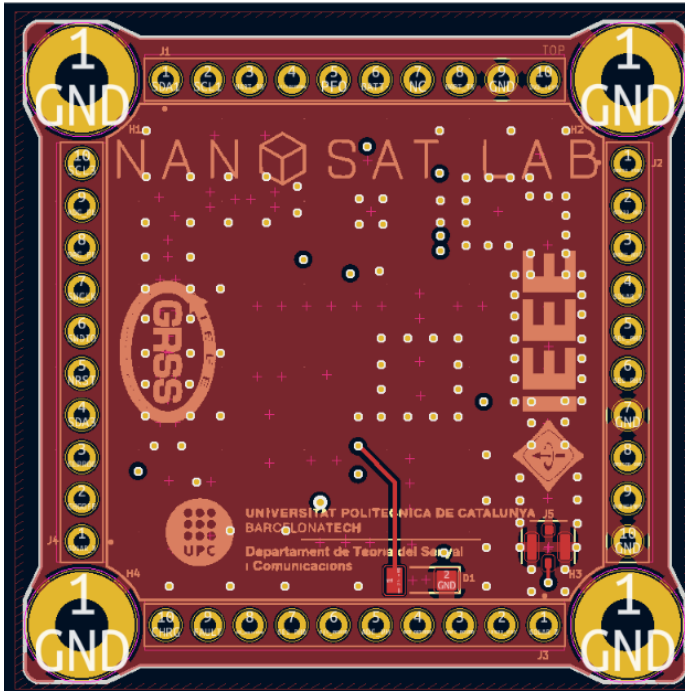
Subsequently, the IF 5'th order **Chebyshev filter** is linked to the tuner's I component differential output. As presented in the Schematic section, it is a differentially matched to $75\ \Omega$ bandpass filter made with discrete components and surrounded again by via RF fencing. To this end, the major design factor was to achieve a balance between component size and track width, as the further apart the pads, the wider the differential track would need to split to connect to them, and the higher the divagation from the required separation obtained previously in the characteristic impedance study. Conversely, the smaller the components, the higher would be the losses, especially in the case of capacitors. However, in the end, as the monolithic series-parallel structure of the filter, combined with the RSSI adaptation network, initially 0604 imperial along with all other biasing elements of the board, exceeded the PCB available space, the decision was made to both reduce the components size to 0402 imperial, as well as to bend the TL taking advantage of the passive components of the filter, action made possible by the low operation frequency of the IF chain.

Moving to the **RSSI**, as mentioned previously, its impedance adaptation network has been structurally integrated within the differential monolith, taking advantage of the identical component format, as well as the straight line formation. Additionally, in terms of biasing elements, the load resistor, as well as the ADC's low pass filter have placed as close as possible in order to better compact the structure, thematic that was employed with all this board's modules

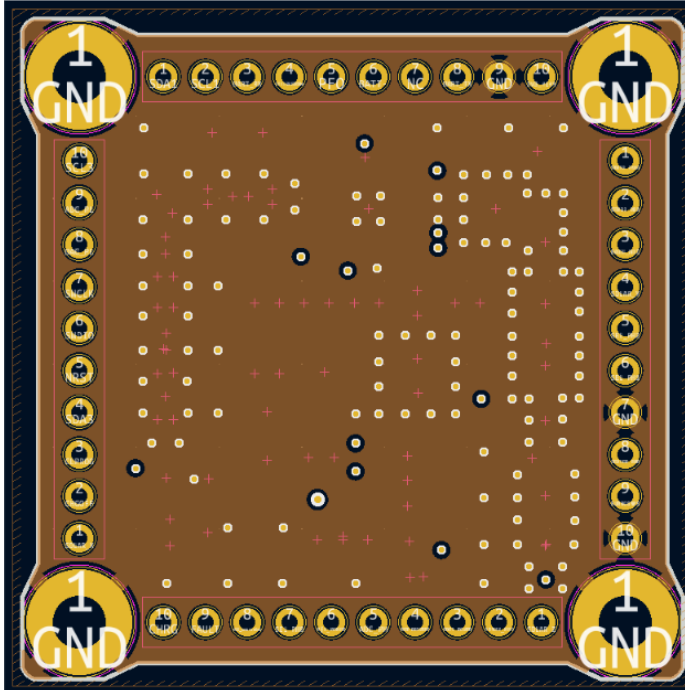
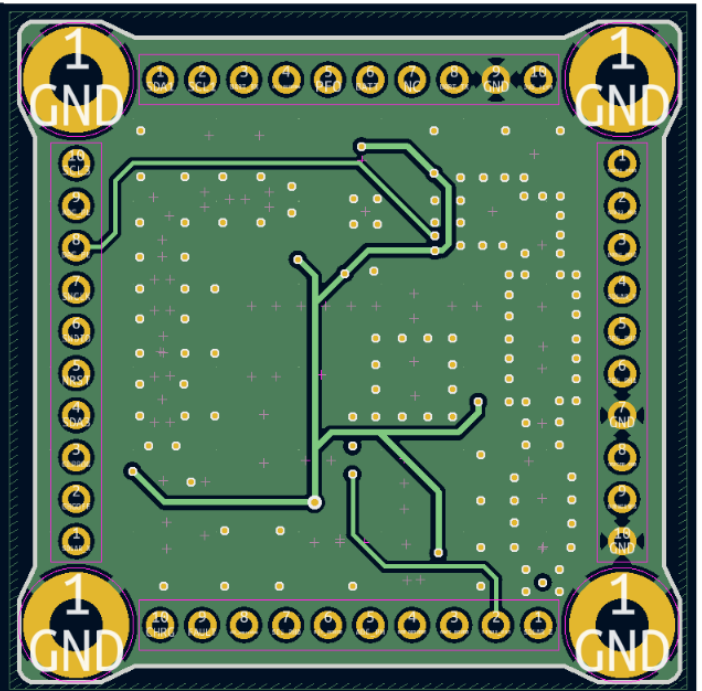
Lastly, the **5V booster and the photodiode opamp** have been designed according to the manufacturer's layout recommendations and placed as possible to their deserving elements: the RF chain LNA and the photodiode respectively.

Finally, the PCB layer views can be revised below, along with some renders of the final assembly:

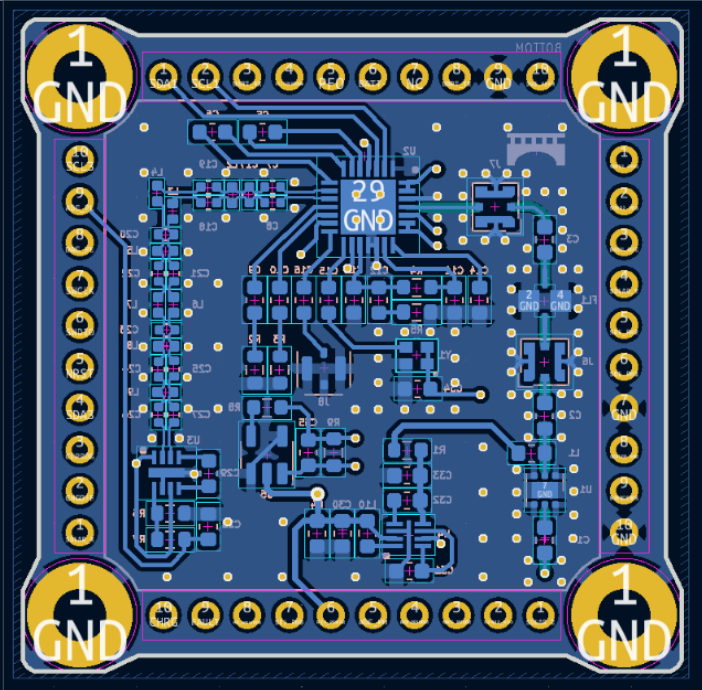
Top layer



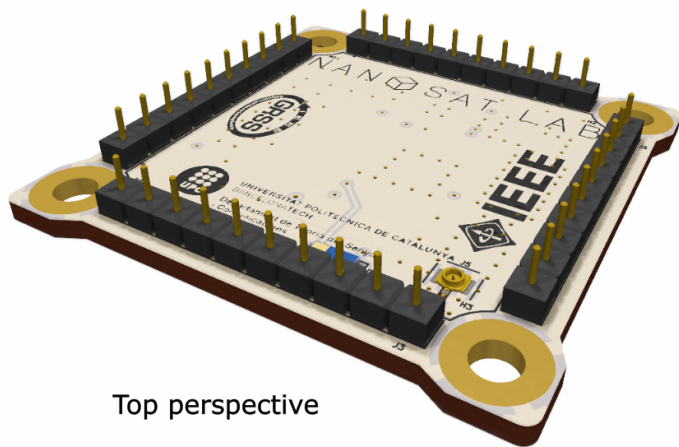
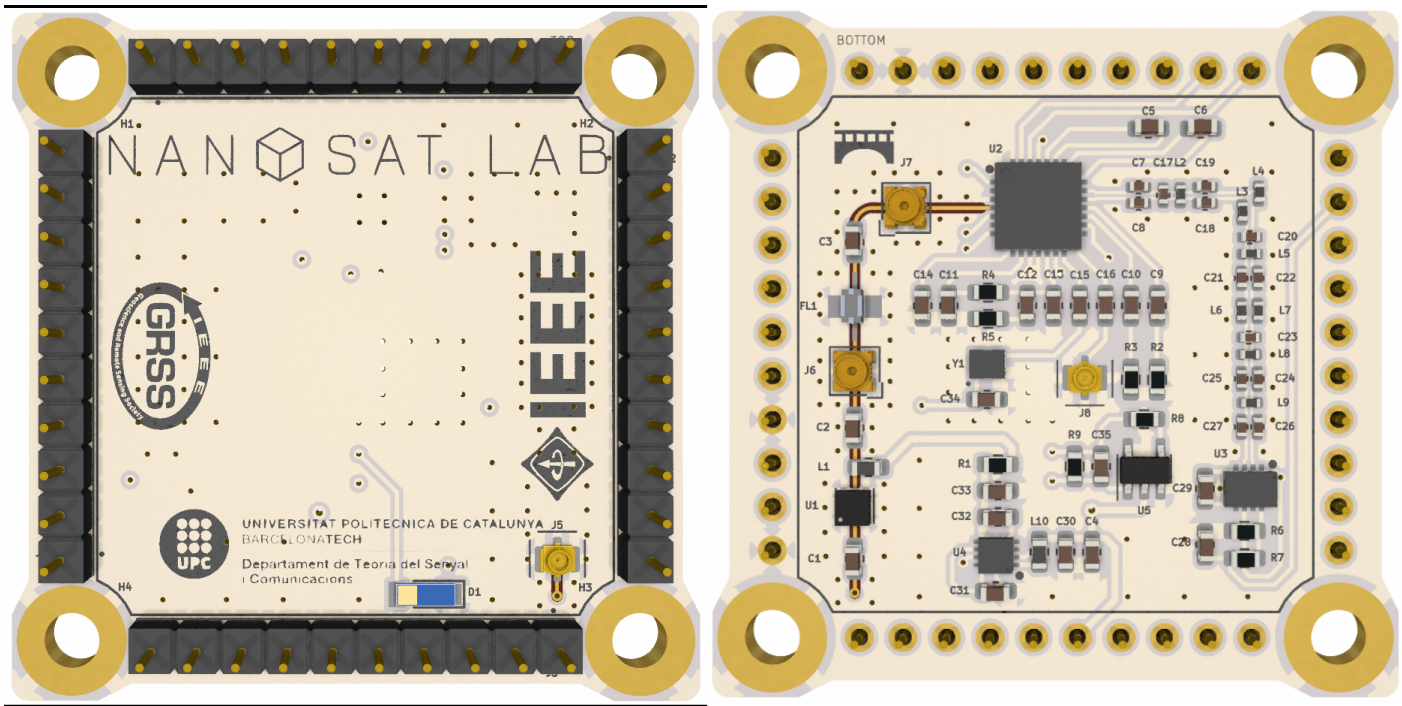
Inner 1 layer



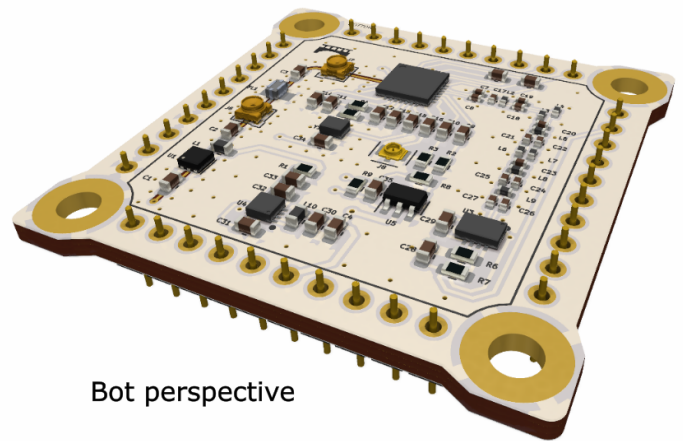
Inner 2 layer



Bottom layer



Top perspective



Bot perspective

Revision #1

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