RFI-5G Payload design

IGARSS_2023_Kband_RFI_Paper.pdf

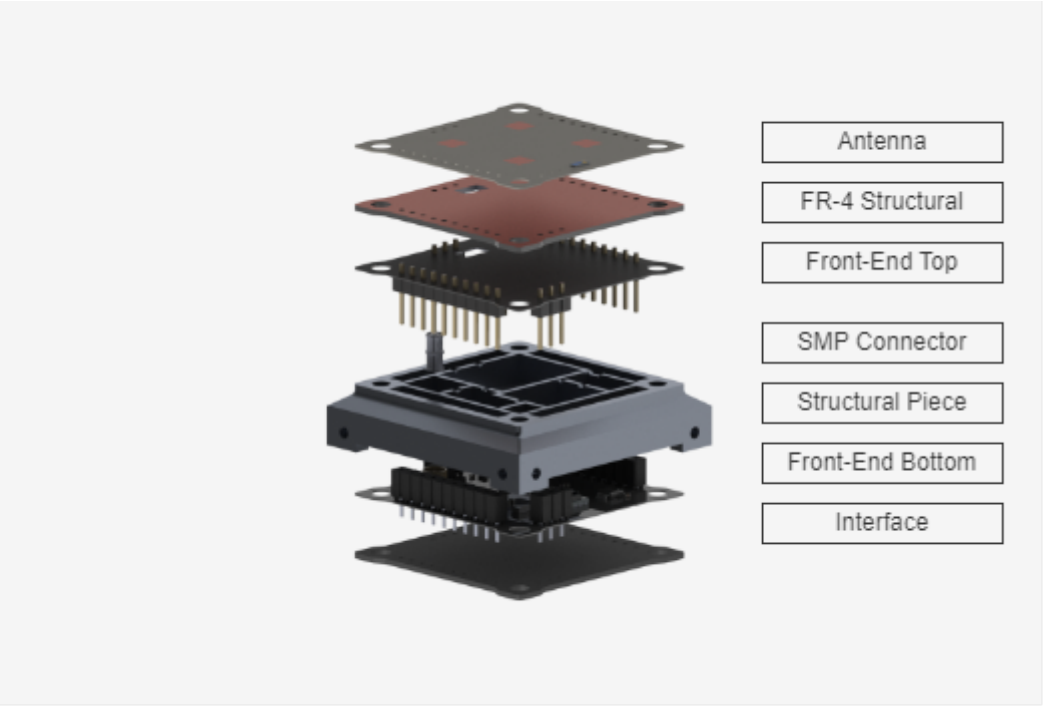
1. Payload Structure

The payload is structured as a vertical stack of PCBs, like the rest of the satellite. This is done in order to be self-contained and to comply with the IEEE Open PocketQube Kit standard.

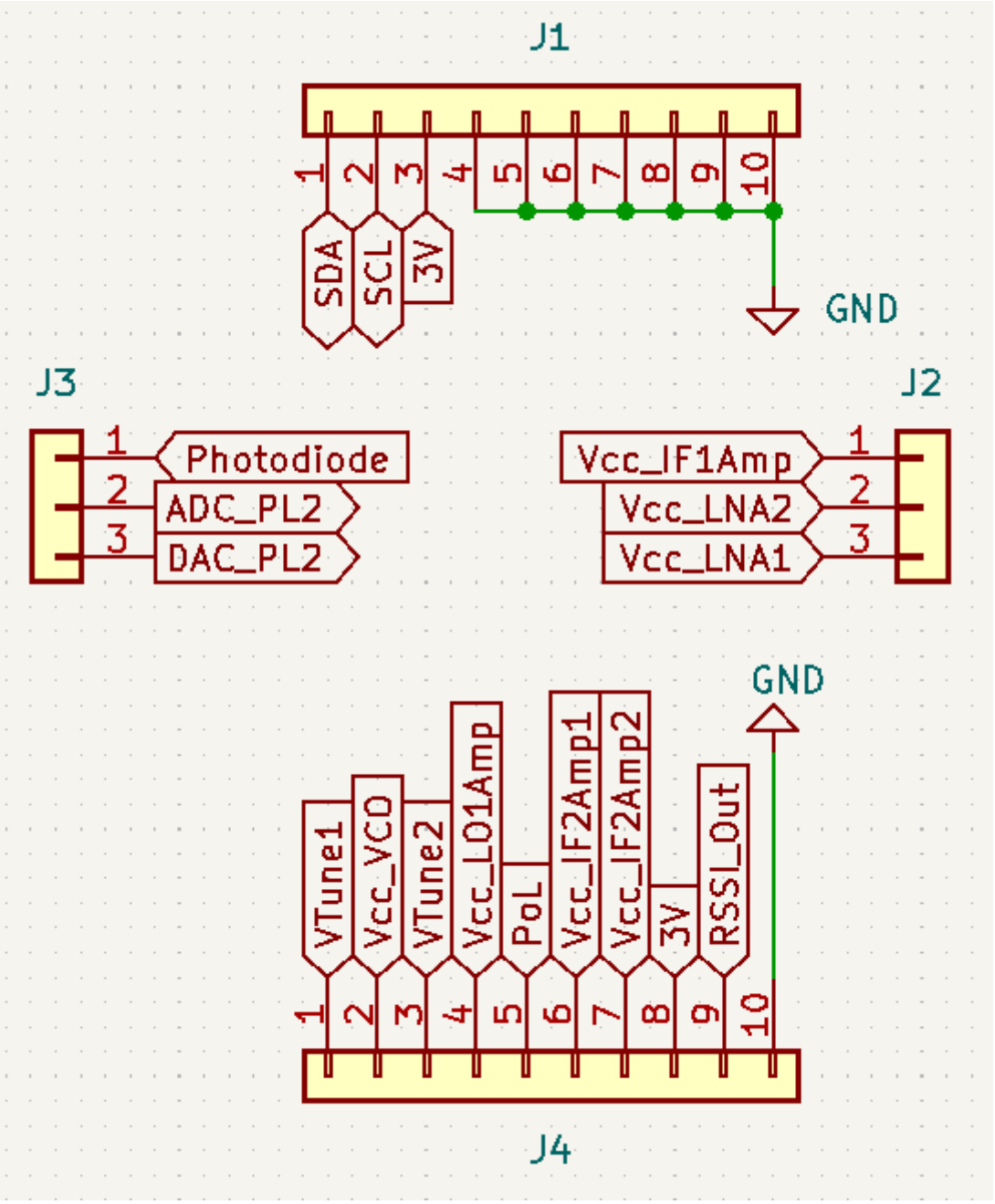
This stack is designed so that the interferences from upper layers cannot penetrate down to the lower side and so the rest of the PocketQube. This isolation is mainly achieved thanks to the Structural piece, the aluminum shield, which connects the grounding from the PCBs in contact with it on both sides, so that it creates a grounded case, creating a Faraday Cage that is able to enclose the interferences radiated from within while also isolating those from the radiation coming from the exterior.

Another relevant structural component is the FR-4 Structural PCB. The only purpose of this PCB is to support the K-Band Antenna, which is very delicate and thin.

In both cases the Antenna and Top PCB with the FR-4 Structural and the Bottom PCB with the Interface they are attached with epoxy glue and soldered pins when possible. This ensures a good rigidity and a proper performance when faced the important vibrations produced during launch.



2. Payload Pinout



3. Schematics

3.1. Interface PCB

The Interface PCB is in charge of doing 3 main things:

- Regulating the voltage from the satellite to provided the needed ones to the different components of the payload.

- Creating a reliable voltage source for the voltage dependant components of the payload such as VCOs.
- Regulating the voltage output from the RSSI block of the payload, ensuring reliable measures.

This is why the interface schematic if divided into three parts.

LDOs

This stage is in charge of regulating the 3.3V voltage line from the PQ to the various required voltage needed in the payload.

Voltage	Target component
2.5V	IF1Amp
2.7V	LNA2
2.75V	
3V	

> To be finished

The schematic below shows the design of the voltage regulation circuit for the payload. The purpose of this circuit is to provide stable, regulated power at various voltage levels required by different components within the payload, which is essential for reliable and accurate signal processing and data collection.

Now an in-depth look at the decisions made in the design will be done:

1. Voltage Regulators (U4 and U5 - MIC2215 Series)

- The MIC2215-AAAYML-TR voltage regulators (U4 and U5) were chosen for their low dropout characteristics and stable output. Low dropout regulators (LDOs) are essential in this design to maintain a consistent voltage output even when the input voltage is only slightly higher than the desired output. This is crucial in space applications or sensitive RF equipment, where power stability impacts the system’s overall performance and noise levels.
- Each LDO is configured to provide a specific voltage level, with U4 supplying one line and U5 supplying another. This setup allows for isolated, stable power lines to reduce cross-interference and ensure that each component receives the necessary voltage.

2. Decoupling Capacitors

- Several capacitors (e.g., C19, C20, C28, etc.) are placed near the voltage regulators and along the power lines to filter out noise and provide a stable DC output. The use of 4.7 µF, 1 µF, and 0.1 µF capacitors at different points serves to filter high-frequency noise and smooth out any power supply variations, a critical step in RF designs where signal integrity can be affected by noise.
- C19 and C32 are examples of capacitors placed close to the MIC2215 regulators, following best practices for power integrity, following the recommended application circuit guidelines provided by the chip manufacturer. These capacitors stabilize the output voltage by providing a reservoir of charge that can quickly respond to changes in load, ensuring the voltage remains stable.

3. Voltage Dividers and Feedback Networks

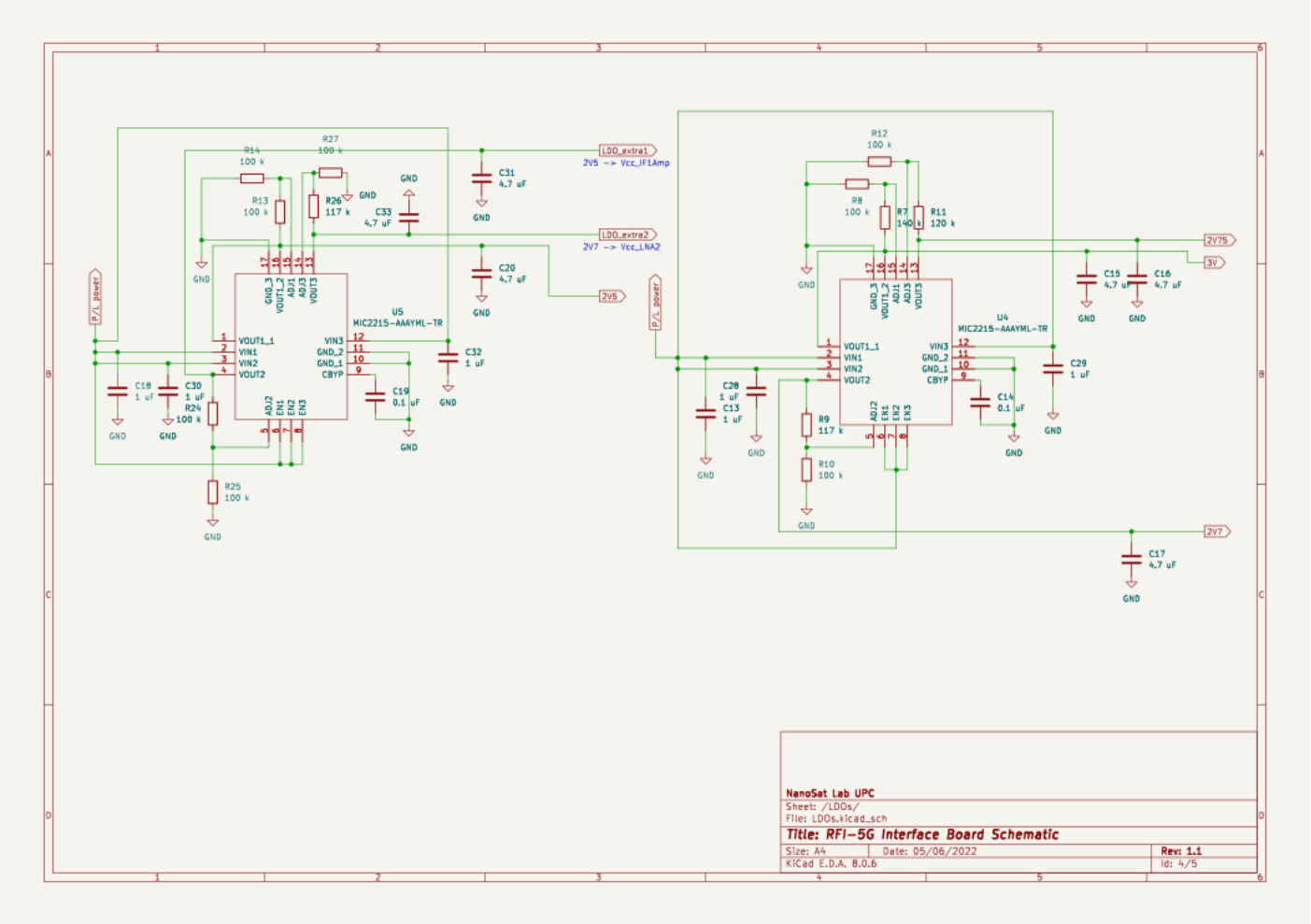
- Resistor networks, such as R9 and R10 for U4 and R25 and R24 for U5, are used to set the output voltages of the LDOs. These resistors form a voltage divider, which provides feedback to the regulator to maintain the correct output level.
- Careful resistor selection here ensures that each voltage line precisely matches the requirements of the connected payload components, which may be sensitive to even minor fluctuations in voltage. For example, some RF components may have strict voltage limits, and a deviation could cause issues in performance or even damage the part.

4. Separate Power Lines for Isolation

- The circuit includes separate voltage lines, labeled LDO_extra1 and LDO_extra2, with respective voltages indicated as 2V5 and 2V7. These lines likely provide power to different

functional blocks within the payload, such as an amplifier (Vcc_IF_Amp) and possibly another component at a similar voltage level but requiring isolation.

- This isolation prevents unwanted interference between different parts of the circuit. In RF designs, where signal fidelity is paramount, isolating power sources for different blocks helps to minimize cross-talk and reduce the risk of interference affecting the sensitive RF signals being processed.



Voltage Boosters

This schematic provides a look at a voltage-boosting circuit. Here, three independent boost converter stages are built around the LT3048IDC-TRMPBF component (U1, U2, and U3). Each of these stages is responsible for generating a specific voltage required by various components in the payload, focusing on boosting an input voltage to a higher, stabilized output for sensitive RF systems.

Here is an expanded explanation of the design decisions and key aspects:

1. Boost Converter ICs (U1, U2, and U3 - LT3048IDC-TRMPBF)

- The LT3048IDC-TRMPBF is a low-noise, high-voltage boost regulator designed to step up an input voltage to a higher output with high efficiency. The choice of this IC is likely due to its high efficiency and ability to handle low-noise applications, which is essential in RF

systems where noise can affect signal quality.
- Each boost converter serves a different voltage rail: LEE1_Vcc, LEE2_Vcc, and 13V. This flexibility allows the system to provide stable, isolated voltage lines to multiple components with distinct power requirements.

2. Input Filtering Components (L1, L2, L3, C24, C25, C27)

- Inductors L1, L2, and L3 (5.6 µH) and input capacitors C24, C25, and C27 (100 nF) are placed at the input of each boost converter to filter the incoming voltage. The inductors help smooth out the current, while the capacitors act as decoupling components to suppress high-frequency noise that could affect the boost conversion process.
- This filtering helps to ensure a clean input voltage, which is crucial for stable and efficient operation of the boost converter. In RF systems, this is especially important to avoid coupling of noise into the RF circuitry, which could degrade signal integrity.

3. Output Voltage Feedback and Resistor Networks

- Each boost converter uses a resistor network (e.g., R1, R2 for U1; R3, R4 for U2; and R5, R6 for U3) to set the output voltage. This resistor network forms a voltage divider that feeds back a portion of the output voltage to the FB (feedback) pin, allowing the converter to regulate the output.
- The precise values of these resistors were chosen to produce the desired output voltages (LEE1_Vcc, LEE2_Vcc, and 13V). Accurate resistor selection is critical to achieve stable, predictable output voltages that match the requirements of the connected components, preventing over-voltage or under-voltage conditions that could affect component performance or even damage them.

4. Output Decoupling and Stabilization (C3, C4, C7, C8, C11, C12)

- Each output line includes decoupling capacitors, with 1 µF and 4.7 µF capacitors (such as C3 and C4 for U1) placed in parallel. The 1 µF capacitor provides low-impedance filtering for high-frequency noise, while the 4.7 µF capacitor smooths out lower-frequency variations and transient currents.
- This dual-capacitor approach improves stability and minimizes ripple on the output lines, which is crucial in RF systems where even minor power fluctuations can affect sensitive signal processing circuits.

5. Bypass Capacitors for Noise Reduction

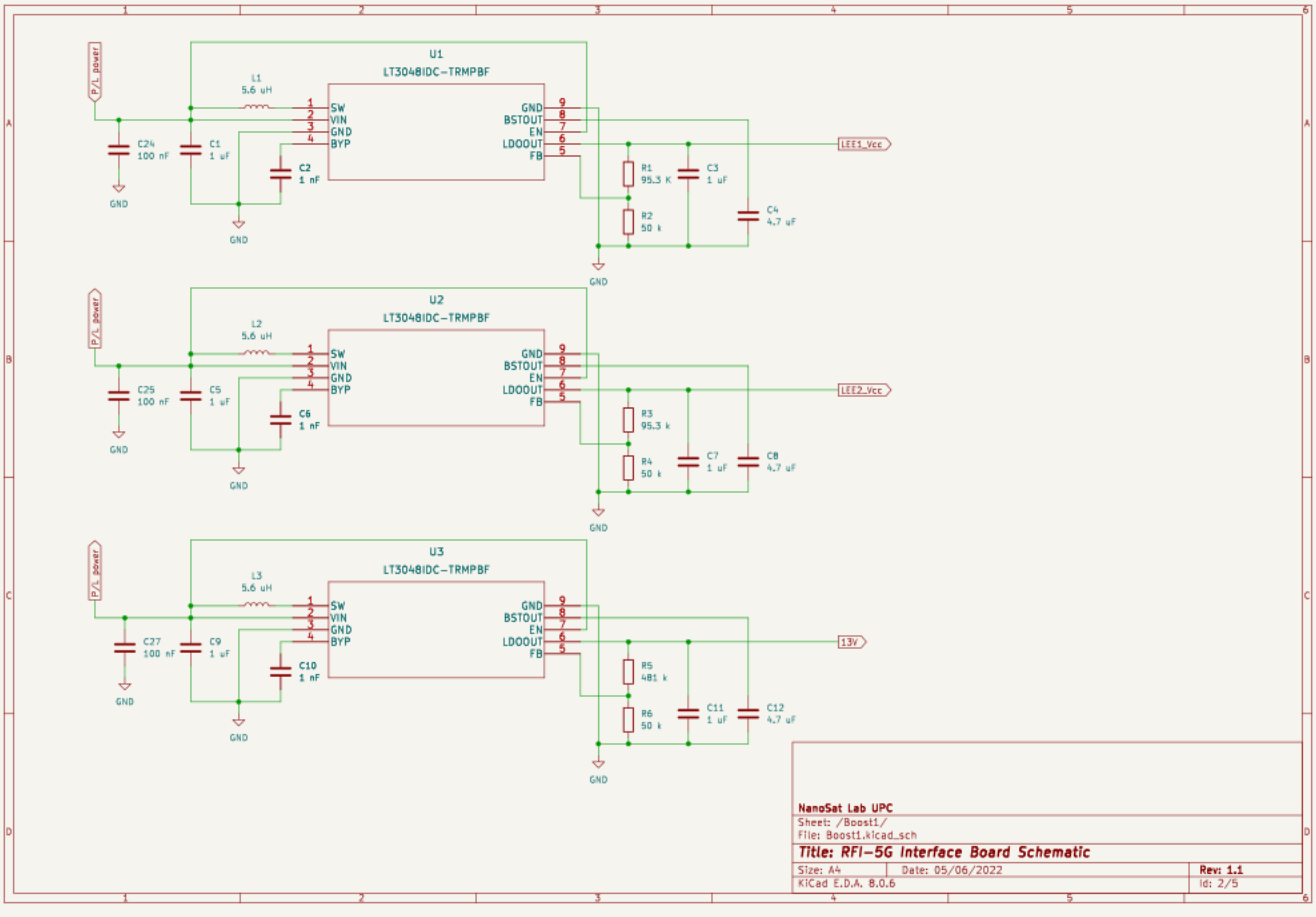
- Small 1 nF capacitors (C2, C6, and C10) are connected to the BYP (bypass) pin of each LT3048 device. These capacitors are used to reduce noise generated by the internal circuitry of the boost converter. The values are chosen according to the manufacturer by following its recommended application circuit.

6. Application-Specific Voltage Rails

- Each voltage line serves a specific purpose, indicated by labels such as LEE1_Vcc, LEE2_Vcc, and 13V. These lines are tailored to the needs of individual components within the RF payload, allowing for optimized power delivery to each functional block.
Voltage Line	Target Component
LEE1_Vcc	
LEE2_Vcc	
13V	
- > Table to be completed

7. Isolation Between Voltage Rails

- By implementing three separate boost converters, the design provides excellent isolation between the various power lines. This is especially beneficial in RF systems where shared power sources could lead to interference and cross-talk between components.
- Each boost converter effectively acts as its own power supply, with independent regulation and filtering, which minimizes the risk of noise or fluctuations affecting multiple components simultaneously.



Instrumentation Amplifier

This schematic shows an instrumentation amplifier stage used to process the voltage output from the RSSI (Received Signal Strength Indicator) block, which holds the scientific data from the payload. The amplifier conditions this signal so that it can be accurately digitized by the DAC input of the satellite's microcontroller.

Below is an expanded explanation of the main components and design choices within this stage:

1. Instrumentation Amplifier (U6 - AD8224ARZ-R7)

- U6 is an AD8224ARZ-R7 instrumentation amplifier, chosen for its precision and low offset, making it ideal for low-level signal measurements. Instrumentation amplifiers are designed to amplify differential signals while rejecting common-mode noise, a key requirement in this setup, where the output from the RSSI might contain noise from other subsystems or the RF environment.
- The amplifier ensures that the RSSI signal can be accurately amplified and fed to the DAC, preserving data integrity and enhancing measurement accuracy for scientific analysis.

2. Gain Resistors (R15, R16, R17, and R18)

- Resistors R15 (11 Ω), R16 (402 kΩ), and R17 (604 kΩ) set the gain of the instrumentation amplifier. The gain configuration allows fine-tuning of the signal amplification to match the input range of the DAC.
- R18 (73.2 Ω) works alongside the feedback network to provide stability and control over the amplifier’s response, ensuring accurate gain with minimal drift, which is essential for scientific measurements.

3. Input and Output Filtering (C21, C22, C26)

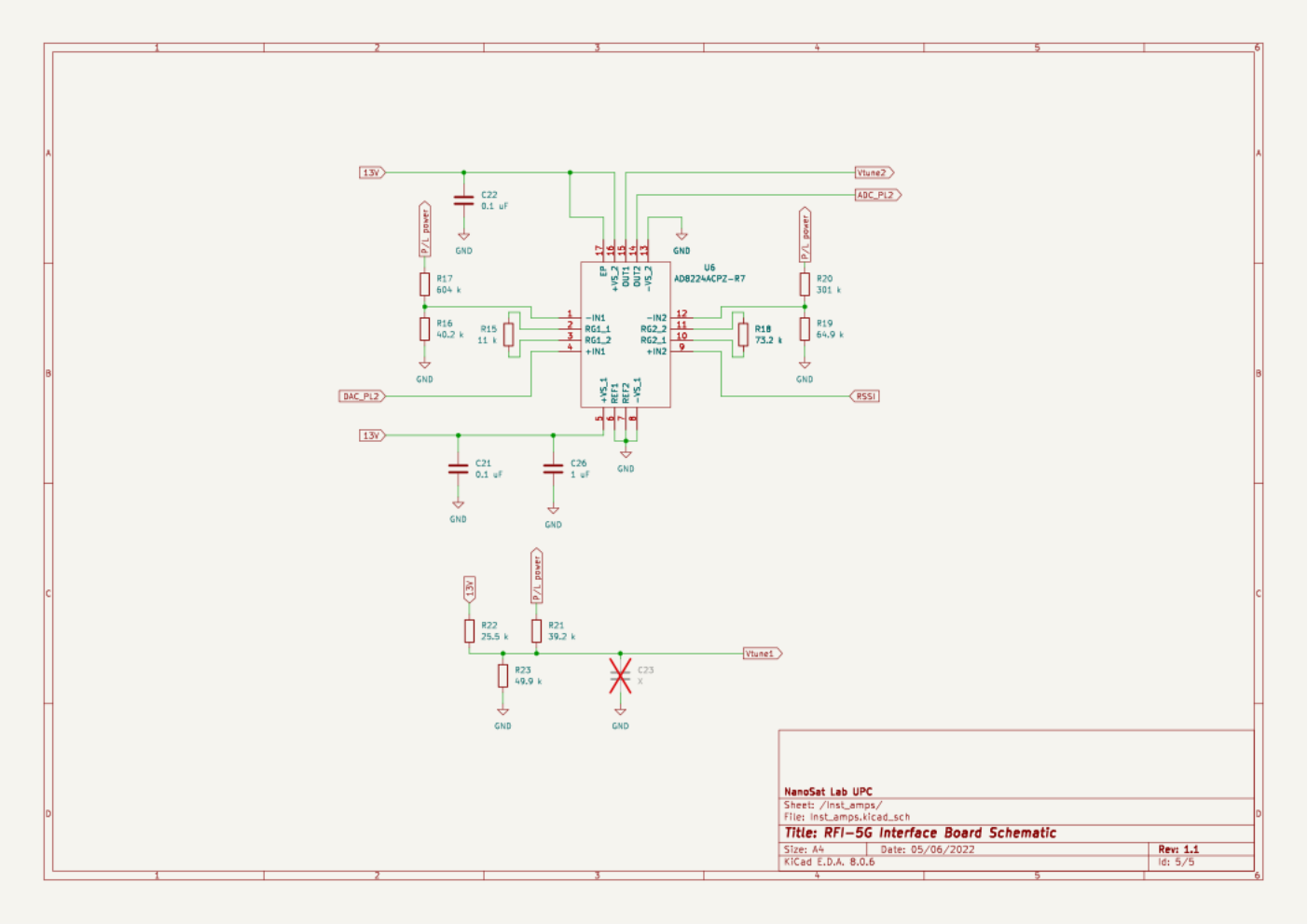
- Capacitors C21 and C22 (both 0.1 µF) are decoupling capacitors that filter out high-frequency noise on the power supply line (13V). Clean power is vital for precision instrumentation amplifiers to avoid fluctuations that could affect amplification accuracy.
- C26 (1 µF) provides additional decoupling on the amplifier's output, further stabilizing the signal before it reaches the DAC. This capacitor helps to smooth out any high-frequency noise that might have coupled through, ensuring a clean, stable signal for digitization.

4. Voltage Divider for Signal Conditioning (R19, R20, R21, R22, R23)

- R19 (64.9 kΩ) and R20 (301 kΩ) form a voltage divider at the amplifier’s output, scaling the amplified signal to the appropriate range for the DAC input.
- Resistors R21 (39.2 kΩ), R22 (255 kΩ), and R23 (49.9 kΩ) form a voltage divider. Also, a voltage divider is used in order to regulate the voltage input to the frist VCO.

5. RSSI Input and Output Connections

- The RSSI label indicates the input connection from the RSSI block, which is a measure of the received signal strength and contains the scientific data output of the payload. The instrumentation amplifier boosts this signal, conditioning it for accurate ADC conversion.
- The amplifier's output is directed toward the DAC_PL2 label, which connects to the DAC input of the satellite’s microcontroller. This connection completes the signal chain from RF reception to digital conversion, allowing the payload’s data to be processed, analyzed, and transmitted.



3.2. Bottom PCB

1. IF Input

- The signal enters the circuit through J5, labeled IF1_in, an SMP connector that receives the IF signal from the previous stage on Top PCB.
- IF1_in then passes through a highpass filter, FL2 (HFCN-5500+), which has a cut-off frequency around 5500 MHz. This filter removes any unwanted signals or noise outside the desired IF band, ensuring only relevant frequencies are processed in the following stages.

2. First Amplification and Bandpass Filtering

- After the highpass filter FL2, the signal is then amplified by U1 (CMD217P5), an RF amplifier. This amplifier boosts the IF signal's strength, improving its signal-to-noise ratio before further processing.
- It is worth mentioning that C1 and C2 (0.33 µF and 100 pF, respectively) are in charge to filter the noise in the voltage line so that the amlifier recieves a clean supply that will not generate further interferences and unnecessary noise.
- After amplification, the signal goes through another lowpass filter, FL1 (LFCW-8400+), with a cut-off frequency around 8400 MHz. This additional filtering stage ensures that the amplified signal remains within the desired frequency range, with any residual out-of-band signals further suppressed.
- The output of this stage is labeled IF1_Out, which carries the filtered and amplified IF signal into the next stage, the mixer.

3. Mixing

> This is the most important part in the payload design

- The IF1_Out signal enters the IF2 section, where it is mixed down to a lower frequency. This is achieved by U2 mixer (model SIN-34+), which combines the incoming IF signal with a LO signal from LO2.
- The mixer's purpose is to produce sum and difference frequencies of the IF1_Out and LO signals. The desired downconverted signal is selected based on the configuration of the circuit, typically choosing the lower frequency (difference) output.
- The LO signal for the mixer is provided through U7 (HMC358), a local oscillator module, generating a stable signal for mixing purposes. This LO frequency is carefully selected to shift the IF signal down to the RSSI bandwith (868MHz).

4. Second Amplification and Filtering

- L3 (120 nH) and C12 (10 nF) form a matching network, which helps optimize the impedance matching between stages to maximize signal transfer and minimize reflections.
- The signal is then amplified by U3 (LT5537), which is another RF amplifier. This amplification ensures that the downconverted signal is strong enough for further processing, particularly since the mixing process may result in signal loss.
- It is worth mentioning that C6 and C7 (1 µF and 10 nF) are in charge to filter the noise in the voltage line so that the amplifier recieves a clean supply that will not generate further interferences and unnecessary noise.

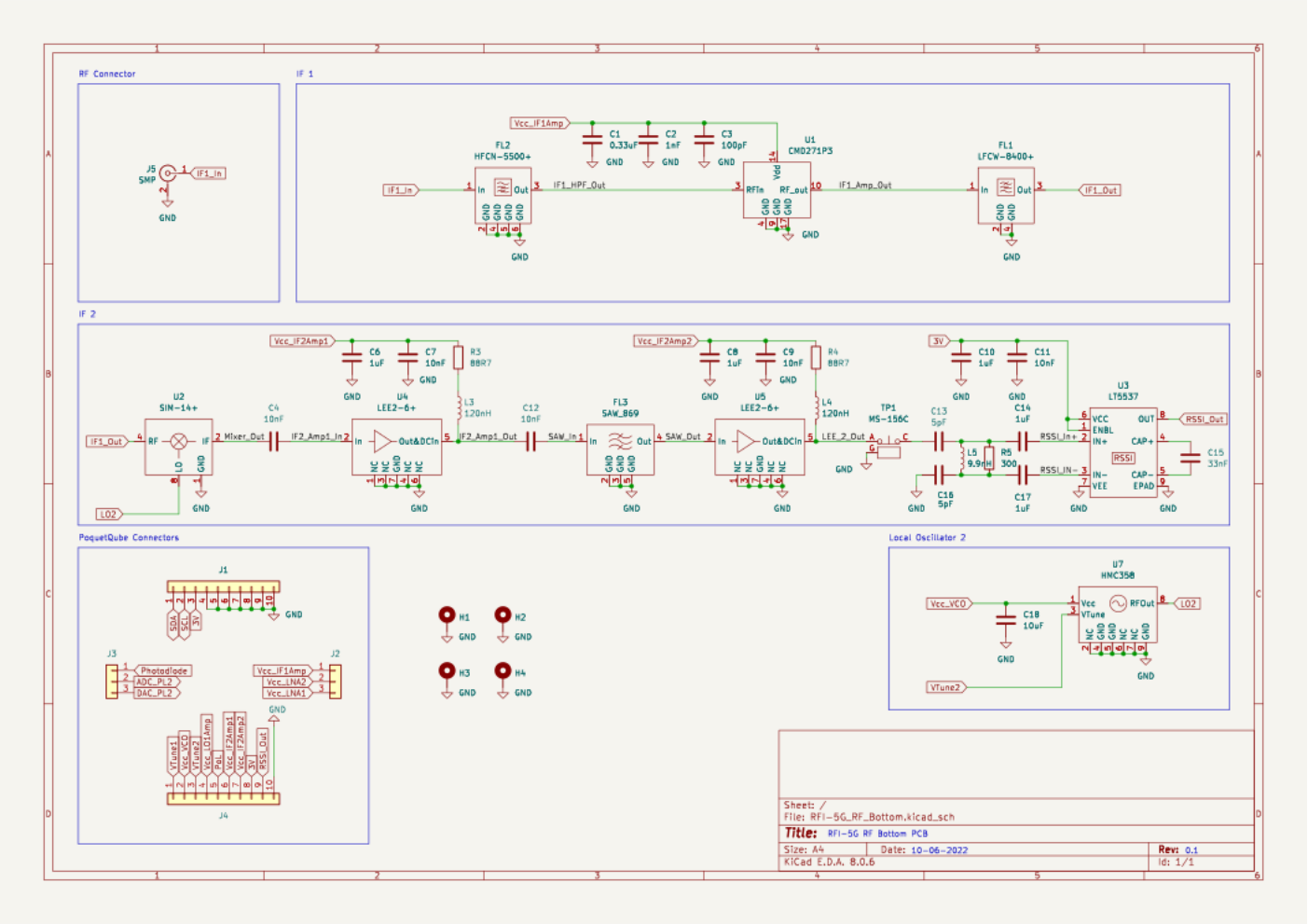
5. Additional Bandpass Filtering (SAW Filter)

- After amplification, the signal goes through FL3 (SAW-669), a SAW (Surface Acoustic Wave) filter with a specified center frequency of 669 MHz. SAW filters are known for their sharp frequency selectivity, providing excellent filtering to eliminate any residual high-frequency components and undesired harmonics.

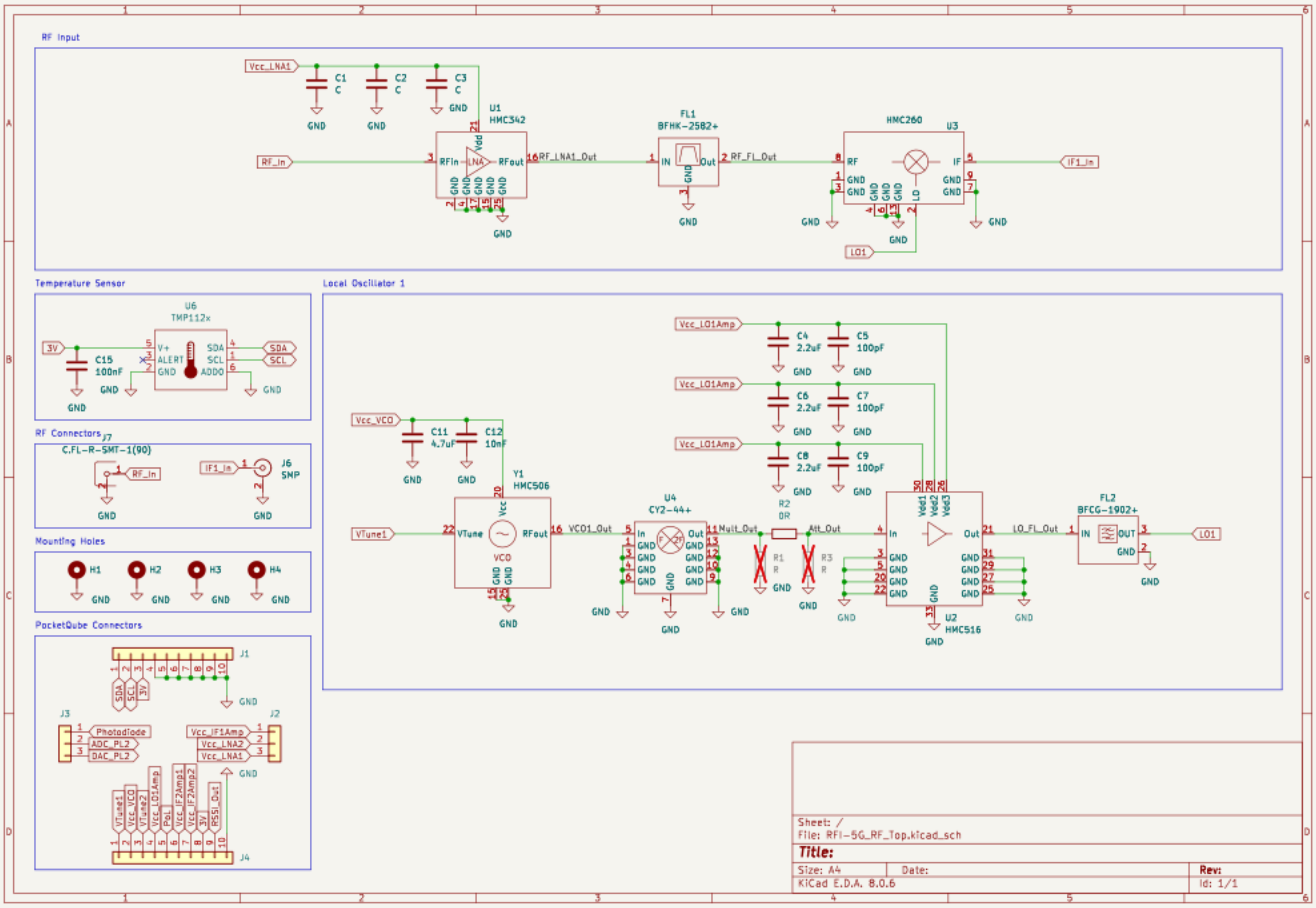
- The filtered signal is output as SAW_Out, which represents a clean, downconverted version of the original IF signal, now at a much lower frequency range, making it easier to handle and digitize in the later stages.

6. RSSI Measurement

- After downconversion, the signal is routed to the RSSI (Received Signal Strength Indicator) section, represented by U3 (LT5537). This IC provides an RSSI output, which gives a DC voltage proportional to the signal strength of the downconverted IF signal.
- The RSSI output is labeled RSSI_Out and is directed to the DAC input of the interface board, which apmplifies this signal and then sends it to the microcontroller in the satellite, allowing real-time monitoring of the received signal strength.
- Capacitors C14 (5 pF), C15 (33 nF), C16 (1 µF), and C17 (1 µF) in the RSSI section provide filtering and stabilization for the RSSI output, ensuring a clean and COHERENT signal for the DAC to measure.



3.3. Top PCB



4. PCBs

This payload is structured in 4 main block as stated in the *Payload block diagram* page. We will start by explaining the Interface PCB.

4.1. Interface PCB

This board is charge of electrically connecting the payload to the rest of the satellite, redistributing the grounding and converting it to a Multiple Point Ground (MPG), more specifically into two points, a single pin on the bottom and a multiple consecutive pin array on the top.

4.2. Bottom PCB

This board takes the IF signal from the Top PCB and downconverts it to be captured by the RSSI and output a voltage proportional to the signal power.

4.3. Top PCB

This board takes the signal from the antenna at the K Band and downconverts it to a Intermediate Frequency (IF).

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