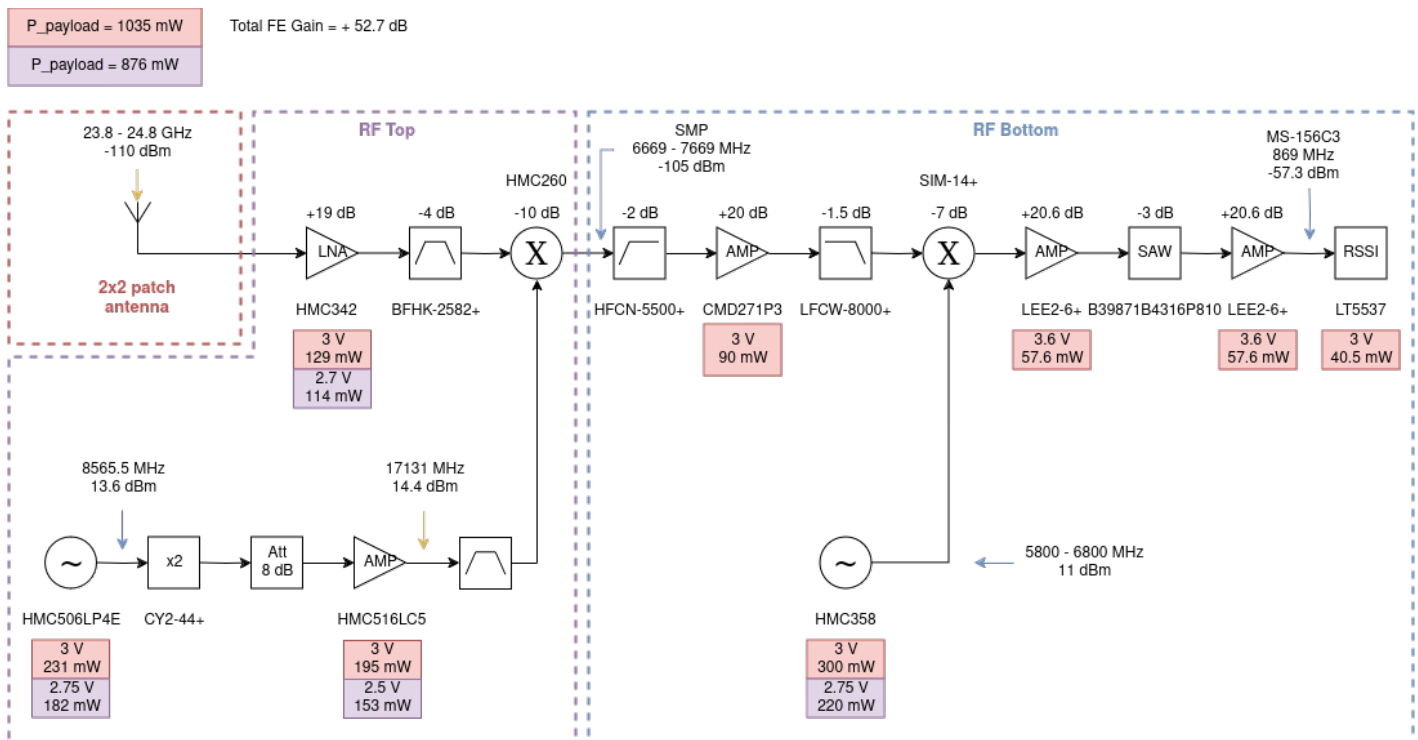# RFI-5G Design

RFI-5G payload designs. Includes electrical, mechanical and software.
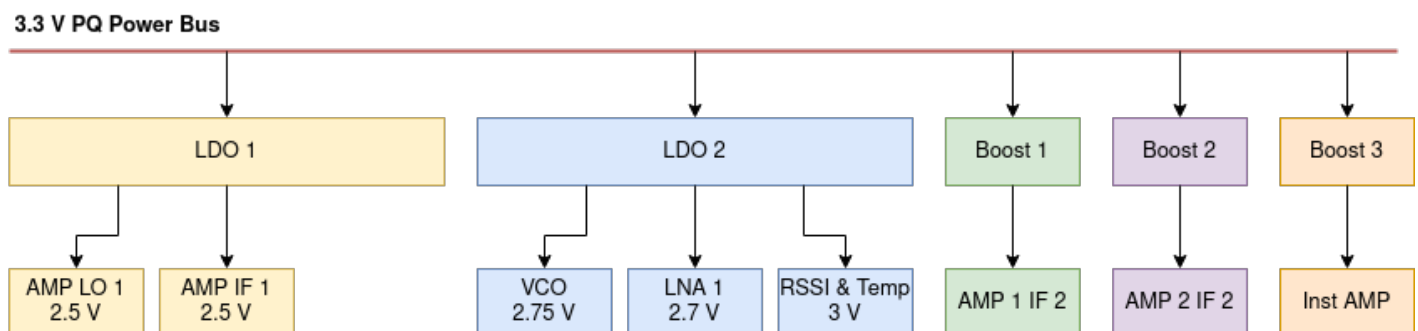
- [RFI-5G Payload block diagrams](#)
- [RFI-5G Payload design](#)
- [Antenna Design](#)
- [Data Acquisition](#)
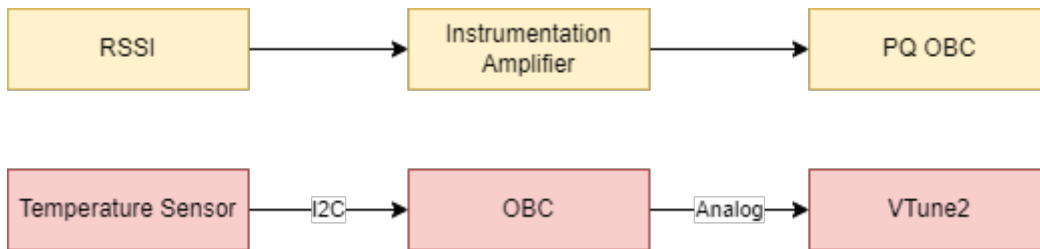- [RFI-Dedicated Thread](#)

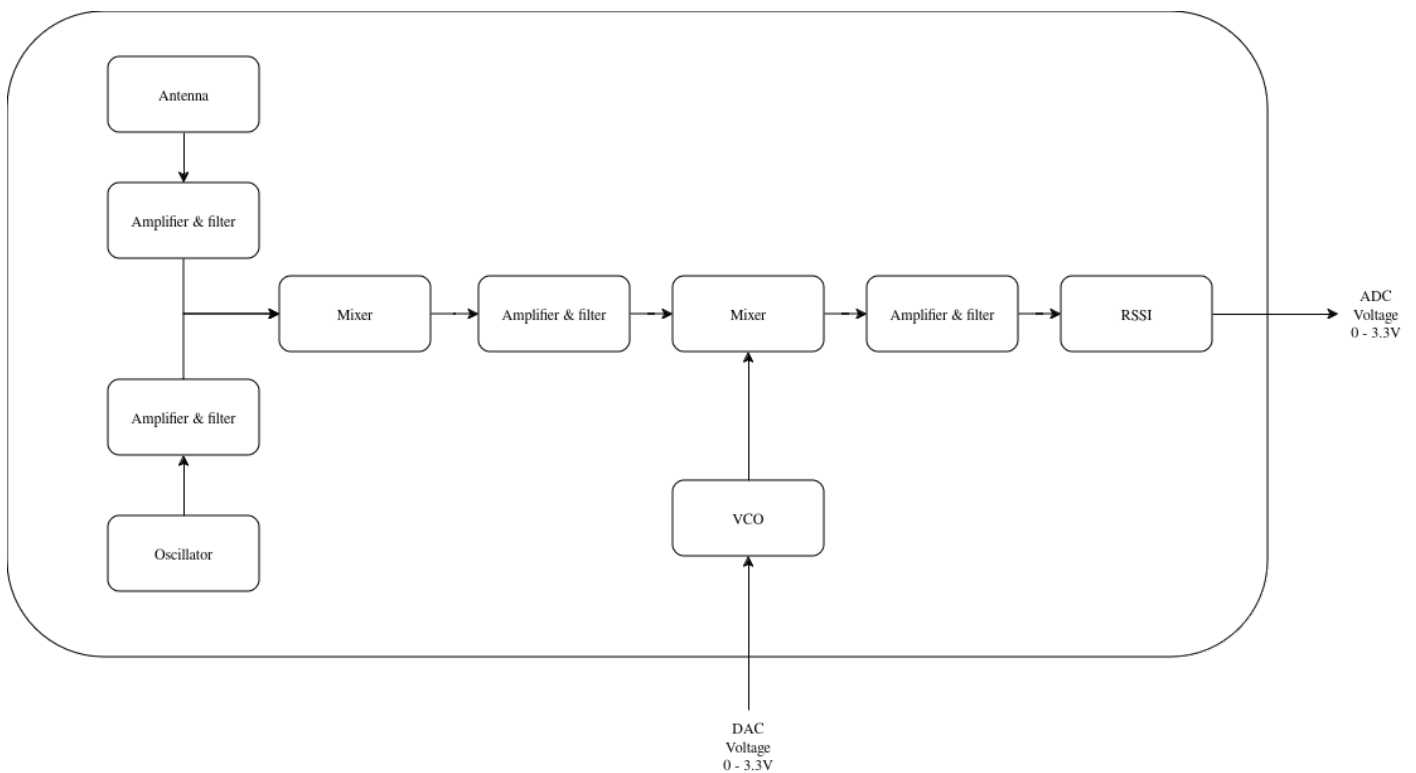# RFI-5G Payload block diagrams

1. FE Block Diagram

2. Power Supply Block Diagram

3. Signal Conditioning Block Diagram

RSSI	→	Instrumentation Amplifier	→	PQ OBC

Temperature Sensor	—I2C→	OBC	—Analog→	VTune2

4. 4. General block diagram

Antenna → Amplifier & filter → Mixer → Amplifier & filter → Mixer → Amplifier & filter → RSSI → ADC Voltage 0 - 3.3V

Oscillator → Amplifier & filter

VCO → Mixer

DAC Voltage 0 - 3.3V → VCO

RFI-5G Payload design
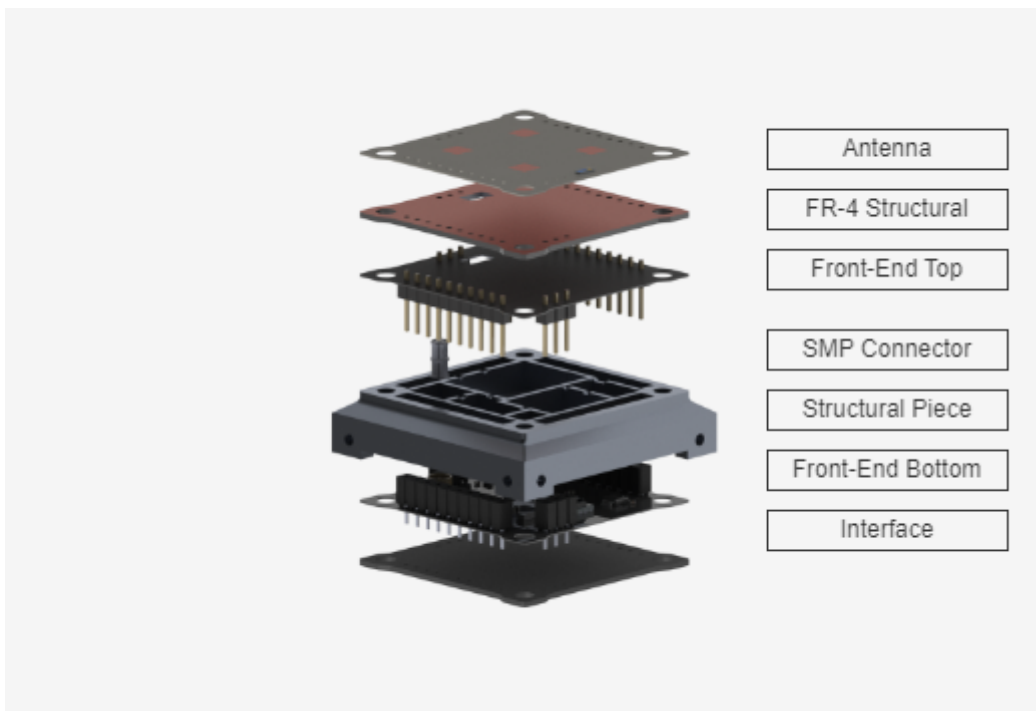
IGARSS_2023_Kband_RFI_Paper.pdf

5. Payload Structure

The payload is structured as a vertical stack of PCBs, like the rest of the satellite. This is done in order to be self-contained and to comply with the IEEE Open PocketQube Kit standard.
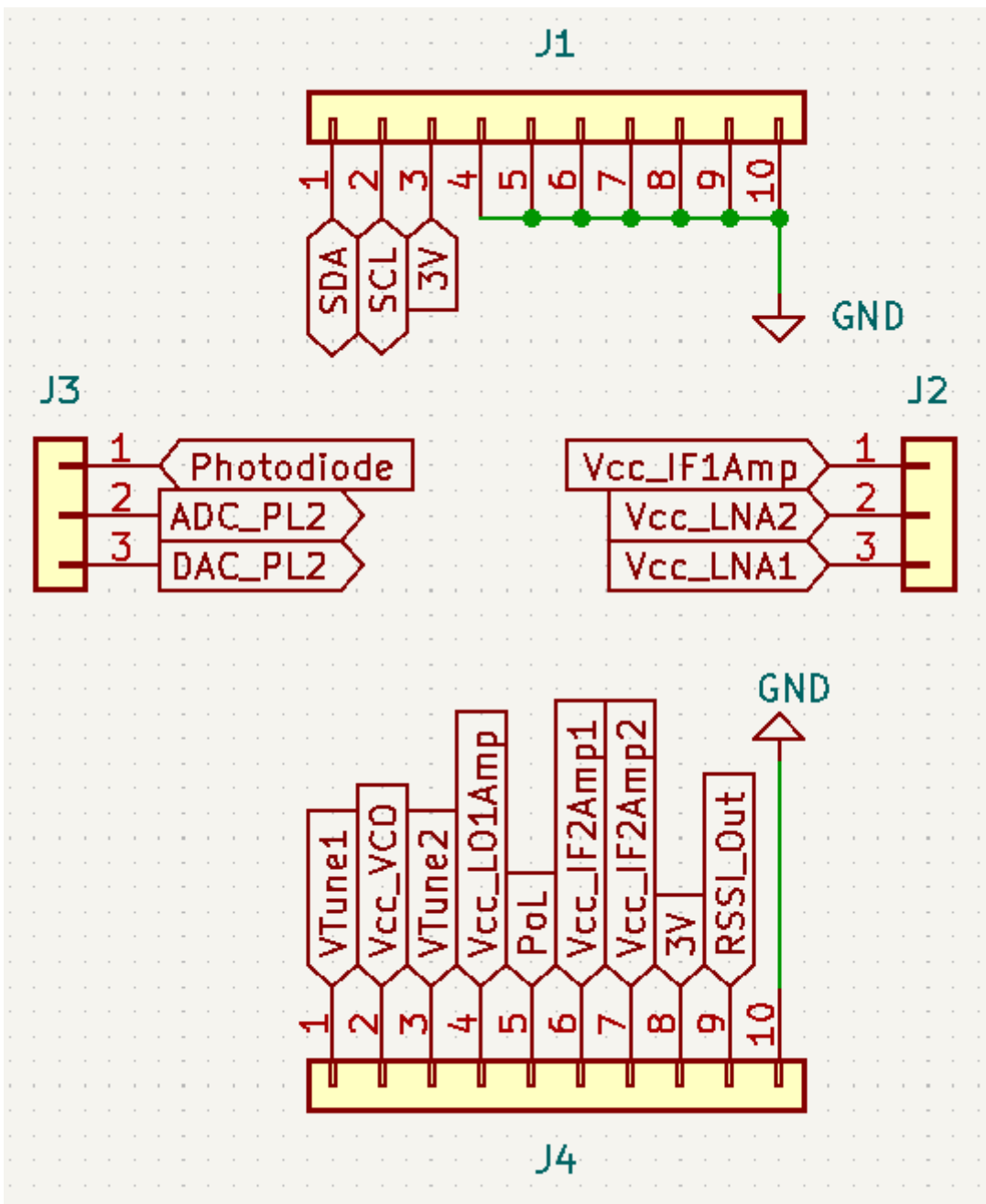
This stack is designed so that the interferences from upper layers cannot penetrate down to the lower side and so the rest of the PocketQube. This isolation is mainly achieved thanks to the Structural piece, the aluminum shield, which connects the grounding from the PCBs in contact with it on both sides, so that it creates a grounded case, creating a Faraday Cage that is able to enclose the interferences radiated from within while also isolating those from the radiation coming from the exterior.

Another relevant structural component is the FR-4 Structural PCB. The only purpose of this PCB is to support the K-Band Antenna, which is very delicate and thin.

In both cases the Antenna and Top PCB with the FR-4 Structural and the Bottom PCB with the Interface they are attached with epoxy glue and soldered pins when possible. This ensures a good rigidity and a proper performance when faced the important vibrations produced during launch.

Antenna

FR-4 Structural

Front-End Top

SMP Connector

Structural Piece

Front-End Bottom

Interface

6. Payload Pinout

7. Schematics

7.1. Interface PCB

The Interface PCB is in charge of doing 3 main things:

- Regulating the voltage from the satellite to provided the needed ones to the different components of the payload.

- Creating a reliable voltage source for the voltage dependant components of the payload such as VCOs.
- Regulating the voltage output from the RSSI block of the payload, ensuring reliable measures.

This is why the interface schematic if divided into three parts.

LDOs

This stage is in charge of regulating the 3.3V voltage line from the PQ to the various required voltage needed in the payload.

Voltage	Target component
2.5V	IF1Amp
2.7V	LNA2
2.75V	
3V	

To be finished

The schematic below shows the design of the voltage regulation circuit for the payload. The purpose of this circuit is to provide stable, regulated power at various voltage levels required by different components within the payload, which is essential for reliable and accurate signal processing and data collection.

Now an in-depth look at the decisions made in the design will be done:

1. Voltage Regulators (U4 and U5 - MIC2215 Series)

- The MIC2215-AAAYML-TR voltage regulators (U4 and U5) were chosen for their low dropout characteristics and stable output. Low dropout regulators (LDOs) are essential in this design to maintain a consistent voltage output even when the input voltage is only slightly higher than the desired output. This is crucial in space applications or sensitive RF equipment, where power stability impacts the system's overall performance and noise levels.
- Each LDO is configured to provide a specific voltage level, with U4 supplying one line and U5 supplying another. This setup allows for isolated, stable power lines to reduce cross-interference and ensure that each component receives the necessary voltage.

2. Decoupling Capacitors

- Several capacitors (e.g., C19, C20, C28, etc.) are placed near the voltage regulators and along the power lines to filter out noise and provide a stable DC output. The use of 4.7 µF, 1 µF, and 0.1 µF capacitors at different points serves to filter high-frequency noise and smooth out any power supply variations, a critical step in RF designs where signal integrity can be affected by noise.
- C19 and C32 are examples of capacitors placed close to the MIC2215 regulators, following best practices for power integrity, following the recommended application circuit guidelines provided by the chip manufacturer. These capacitors stabilize the output voltage by providing a reservoir of charge that can quickly respond to changes in load, ensuring the voltage remains stable.

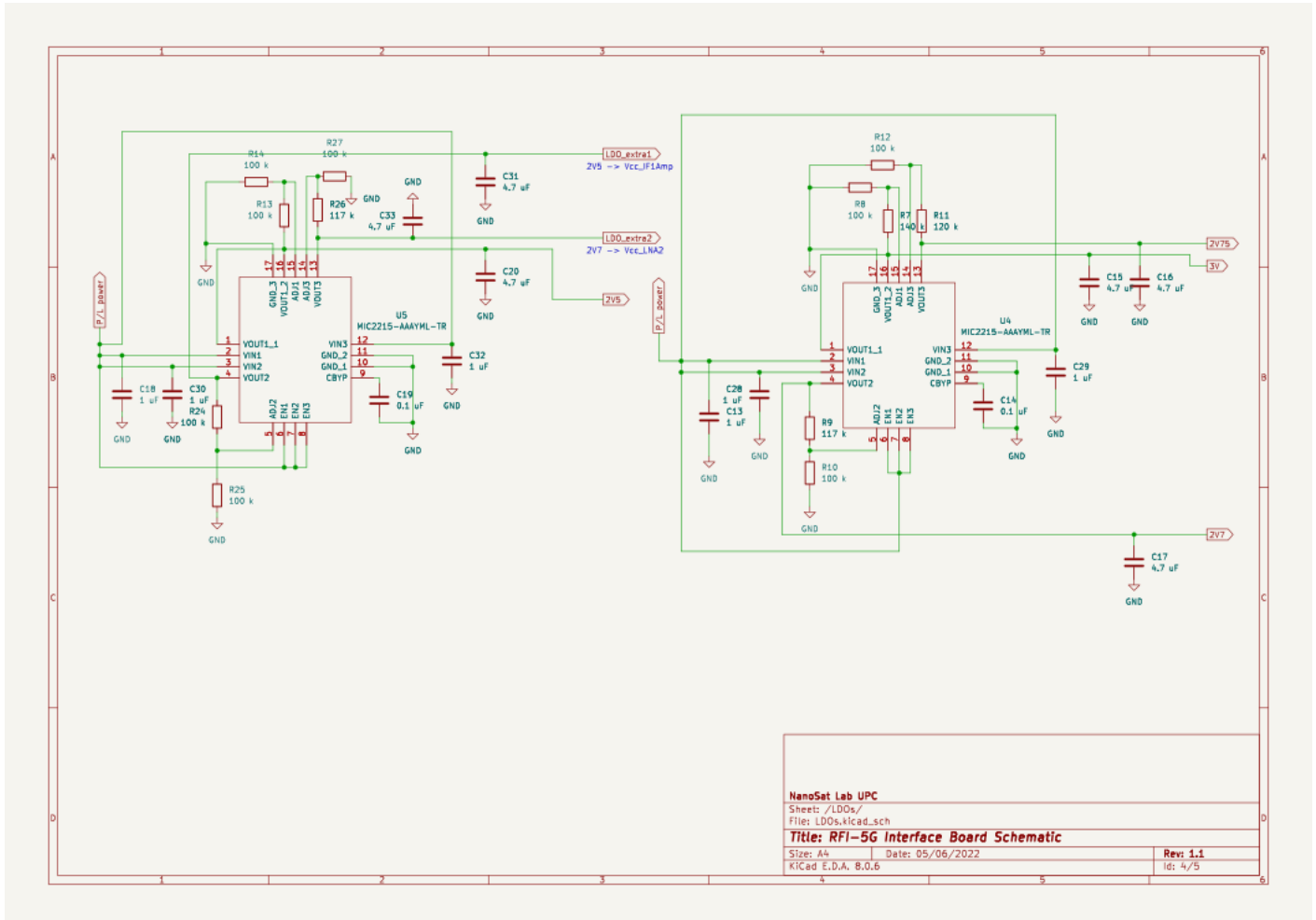## 3. Voltage Dividers and Feedback Networks

- Resistor networks, such as R9 and R10 for U4 and R25 and R24 for U5, are used to set the output voltages of the LDOs. These resistors form a voltage divider, which provides feedback to the regulator to maintain the correct output level.
- Careful resistor selection here ensures that each voltage line precisely matches the requirements of the connected payload components, which may be sensitive to even minor fluctuations in voltage. For example, some RF components may have strict voltage limits, and a deviation could cause issues in performance or even damage the part.

4. Separate Power Lines for Isolation

- The circuit includes separate voltage lines, labeled LDO_extra1 and LDO_extra2, with respective voltages indicated as 2V5 and 2V7. These lines likely provide power to different

functional blocks within the payload, such as an amplifier (Vcc_IF_Amp) and possibly another component at a similar voltage level but requiring isolation.

- This isolation prevents unwanted interference between different parts of the circuit. In RF designs, where signal fidelity is paramount, isolating power sources for different blocks helps to minimize cross-talk and reduce the risk of interference affecting the sensitive RF signals being processed.

Voltage Boosters

This schematic provides a look at a voltage-boosting circuit. Here, three independent boost converter stages are built around the LT3048IDC-TRMPBF component (U1, U2, and U3). Each of these stages is responsible for generating a specific voltage required by various components in the payload, focusing on boosting an input voltage to a higher, stabilized output for sensitive RF systems.

Here is an expanded explanation of the design decisions and key aspects:

1. Boost Converter ICs (U1, U2, and U3 - LT3048IDC-TRMPBF)

- The LT3048IDC-TRMPBF is a low-noise, high-voltage boost regulator designed to step up an input voltage to a higher output with high efficiency. The choice of this IC is likely due to its high efficiency and ability to handle low-noise applications, which is essential in RF

systems where noise can affect signal quality.

- Each boost converter serves a different voltage rail: LEE1_Vcc, LEE2_Vcc, and 13V. This flexibility allows the system to provide stable, isolated voltage lines to multiple components with distinct power requirements.

2. Input Filtering Components (L1, L2, L3, C24, C25, C27)

- Inductors L1, L2, and L3 (5.6 µH) and input capacitors C24, C25, and C27 (100 nF) are placed at the input of each boost converter to filter the incoming voltage. The inductors help smooth out the current, while the capacitors act as decoupling components to suppress high-frequency noise that could affect the boost conversion process.
- This filtering helps to ensure a clean input voltage, which is crucial for stable and efficient operation of the boost converter. In RF systems, this is especially important to avoid coupling of noise into the RF circuitry, which could degrade signal integrity.

3. Output Voltage Feedback and Resistor Networks

- Each boost converter uses a resistor network (e.g., R1, R2 for U1; R3, R4 for U2; and R5, R6 for U3) to set the output voltage. This resistor network forms a voltage divider that feeds back a portion of the output voltage to the FB (feedback) pin, allowing the converter to regulate the output.
- The precise values of these resistors were chosen to produce the desired output voltages (LEE1_Vcc, LEE2_Vcc, and 13V). Accurate resistor selection is critical to achieve stable, predictable output voltages that match the requirements of the connected components, preventing over-voltage or under-voltage conditions that could affect component performance or even damage them.

4. Output Decoupling and Stabilization (C3, C4, C7, C8, C11, C12)

- Each output line includes decoupling capacitors, with 1 µF and 4.7 µF capacitors (such as C3 and C4 for U1) placed in parallel. The 1 µF capacitor provides low-impedance filtering for high-frequency noise, while the 4.7 µF capacitor smooths out lower-frequency variations and transient currents.
- This dual-capacitor approach improves stability and minimizes ripple on the output lines, which is crucial in RF systems where even minor power fluctuations can affect sensitive signal processing circuits.

5. Bypass Capacitors for Noise Reduction

- Small 1 nF capacitors (C2, C6, and C10) are connected to the BYP (bypass) pin of each LT3048 device. These capacitors are used to reduce noise generated by the internal circuitry of the boost converter. The values are chosen according to the manufacturer by following its recommended application circuit.

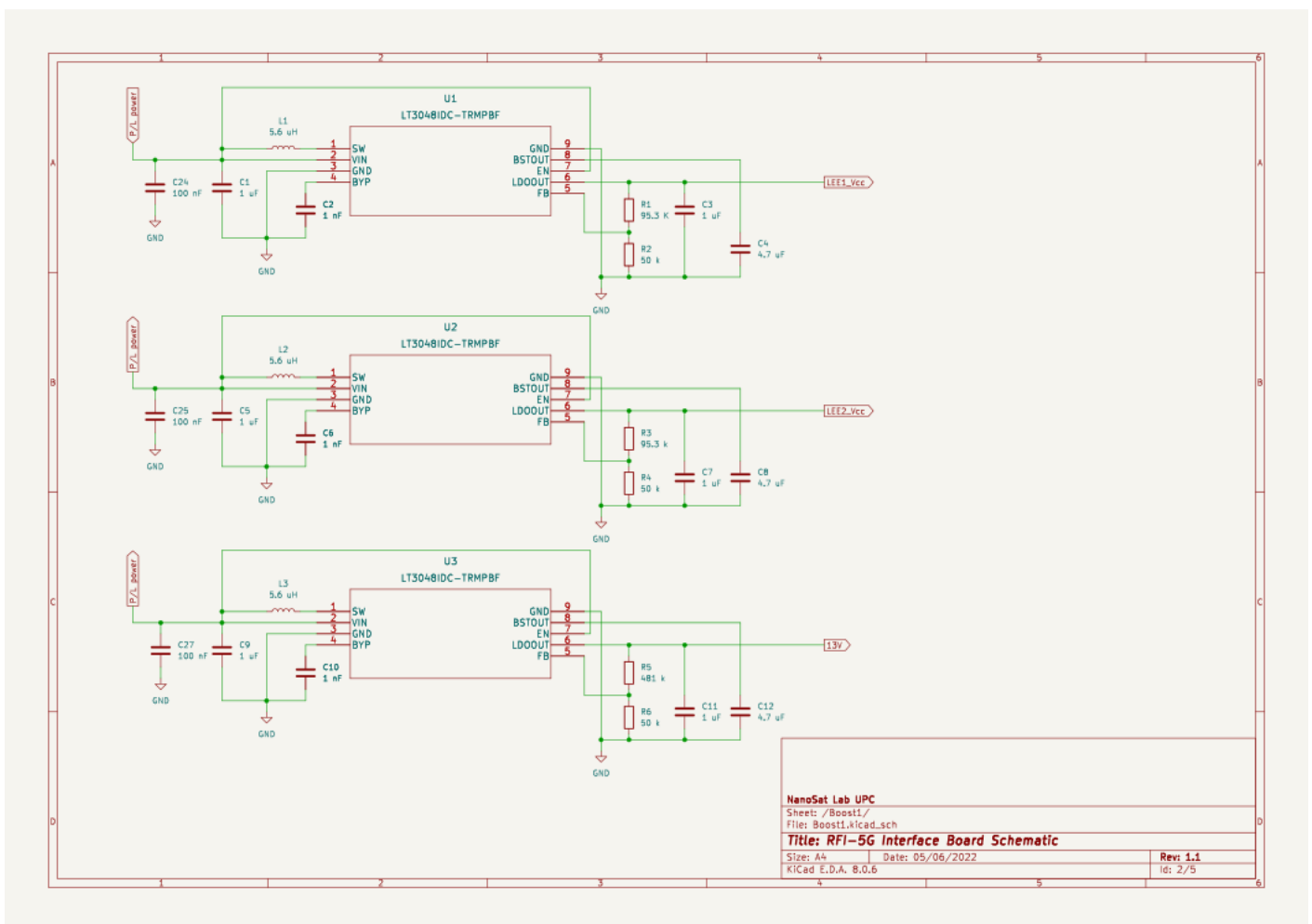## 6. Application-Specific Voltage Rails

- Each voltage line serves a specific purpose, indicated by labels such as LEE1_Vcc, LEE2_Vcc, and 13V. These lines are tailored to the needs of individual components within the RF payload, allowing for optimized power delivery to each functional block.

Voltage Line	Target Component
LEE1_Vcc	
LEE2_Vcc	
13V	

- Table to be completed

7. Isolation Between Voltage Rails

- By implementing three separate boost converters, the design provides excellent isolation between the various power lines. This is especially beneficial in RF systems where shared power sources could lead to interference and cross-talk between components.
- Each boost converter effectively acts as its own power supply, with independent regulation and filtering, which minimizes the risk of noise or fluctuations affecting multiple components simultaneously.

Instrumentation Amplifier

This schematic shows an instrumentation amplifier stage used to process the voltage output from the RSSI (Received Signal Strength Indicator) block, which holds the scientific data from the payload. The amplifier conditions this signal so that it can be accurately digitized by the DAC input of the satellite's microcontroller.

Below is an expanded explanation of the main components and design choices within this stage:

1. Instrumentation Amplifier (U6 - AD8224ARZ-R7)

- U6 is an AD8224ARZ-R7 instrumentation amplifier, chosen for its precision and low offset, making it ideal for low-level signal measurements. Instrumentation amplifiers are designed to amplify differential signals while rejecting common-mode noise, a key requirement in this setup, where the output from the RSSI might contain noise from other subsystems or the RF environment.
- The amplifier ensures that the RSSI signal can be accurately amplified and fed to the DAC, preserving data integrity and enhancing measurement accuracy for scientific analysis.

2. Gain Resistors (R15, R16, R17, and R18)

- Resistors R15 (11 Ω), R16 (402 kΩ), and R17 (604 kΩ) set the gain of the instrumentation amplifier. The gain configuration allows fine-tuning of the signal amplification to match the input range of the DAC.
- R18 (73.2 Ω) works alongside the feedback network to provide stability and control over the amplifier's response, ensuring accurate gain with minimal drift, which is essential for scientific measurements.

3. Input and Output Filtering (C21, C22, C26)

- Capacitors C21 and C22 (both 0.1 µF) are decoupling capacitors that filter out high-frequency noise on the power supply line (13V). Clean power is vital for precision instrumentation amplifiers to avoid fluctuations that could affect amplification accuracy.
- C26 (1 µF) provides additional decoupling on the amplifier's output, further stabilizing the signal before it reaches the DAC. This capacitor helps to smooth out any high-frequency noise that might have coupled through, ensuring a clean, stable signal for digitization.

4. Voltage Divider for Signal Conditioning (R19, R20, R21, R22, R23)

- R19 (64.9 kΩ) and R20 (301 kΩ) form a voltage divider at the amplifier's output, scaling the amplified signal to the appropriate range for the DAC input.
- Resistors R21 (39.2 kΩ), R22 (255 kΩ), and R23 (49.9 kΩ) form a voltage divider. Also, a voltage divider is used in order to regulate the voltage input to the frist VCO.

5. RSSI Input and Output Connections

- The RSSI label indicates the input connection from the RSSI block, which is a measure of the received signal strength and contains the scientific data output of the payload. The instrumentation amplifier boosts this signal, conditioning it for accurate ADC conversion.
- The amplifier's output is directed toward the DAC_PL2 label, which connects to the DAC input of the satellite's microcontroller. This connection completes the signal chain from RF reception to digital conversion, allowing the payload's data to be processed, analyzed, and transmitted.

7.2. Bottom PCB

1. IF Input

- The signal enters the circuit through J5, labeled IF1_in, an SMP connector that receives the IF signal from the previous stage on Top PCB.
- IF1_in then passes through a highpass filter, FL2 (HFCN-5500+), which has a cut-off frequency around 5500 MHz. This filter removes any unwanted signals or noise outside the desired IF band, ensuring only relevant frequencies are processed in the following stages.

2. First Amplification and Bandpass Filtering

- After the highpass filter FL2, the signal is then amplified by U1 (CMD217P5), an RF amplifier. This amplifier boosts the IF signal's strength, improving its signal-to-noise ratio before further processing.
- It is worth mentioning that C1 and C2 (0.33 µF and 100 pF, respectively) are in charge to filter the noise in the voltage line so that the amlifier recieves a clean supply that will not generate further interferences and unnecessary noise.
- After amplification, the signal goes through another lowpass filter, FL1 (LFCW-8400+), with a cut-off frequency around 8400 MHz. This additional filtering stage ensures that the amplified signal remains within the desired frequency range, with any residual out-of-band signals further suppressed.
- The output of this stage is labeled IF1_Out, which carries the filtered and amplified IF signal into the next stage, the mixer.

3. Mixing

> This is the most important part in the payload design

- The IF1_Out signal enters the IF2 section, where it is mixed down to a lower frequency. This is achieved by U2 mixer (model SIN-34+), which combines the incoming IF signal with a LO signal from LO2.
- The mixer's purpose is to produce sum and difference frequencies of the IF1_Out and LO signals. The desired downconverted signal is selected based on the configuration of the circuit, typically choosing the lower frequency (difference) output.
- The LO signal for the mixer is provided through U7 (HMC358), a local oscillator module, generating a stable signal for mixing purposes. This LO frequency is carefully selected to shift the IF signal down to the RSSI bandwith (868MHz).

4. Second Amplification and Filtering

- L3 (120 nH) and C12 (10 nF) form a matching network, which helps optimize the impedance matching between stages to maximize signal transfer and minimize reflections.
- The signal is then amplified by U3 (LT5537), which is another RF amplifier. This amplification ensures that the downconverted signal is strong enough for further processing, particularly since the mixing process may result in signal loss.
- It is worth mentioning that C6 and C7 (1 µF and 10 nF) are in charge to filter the noise in the voltage line so that the amplifier recieves a clean supply that will not generate further interferences and unnecessary noise.
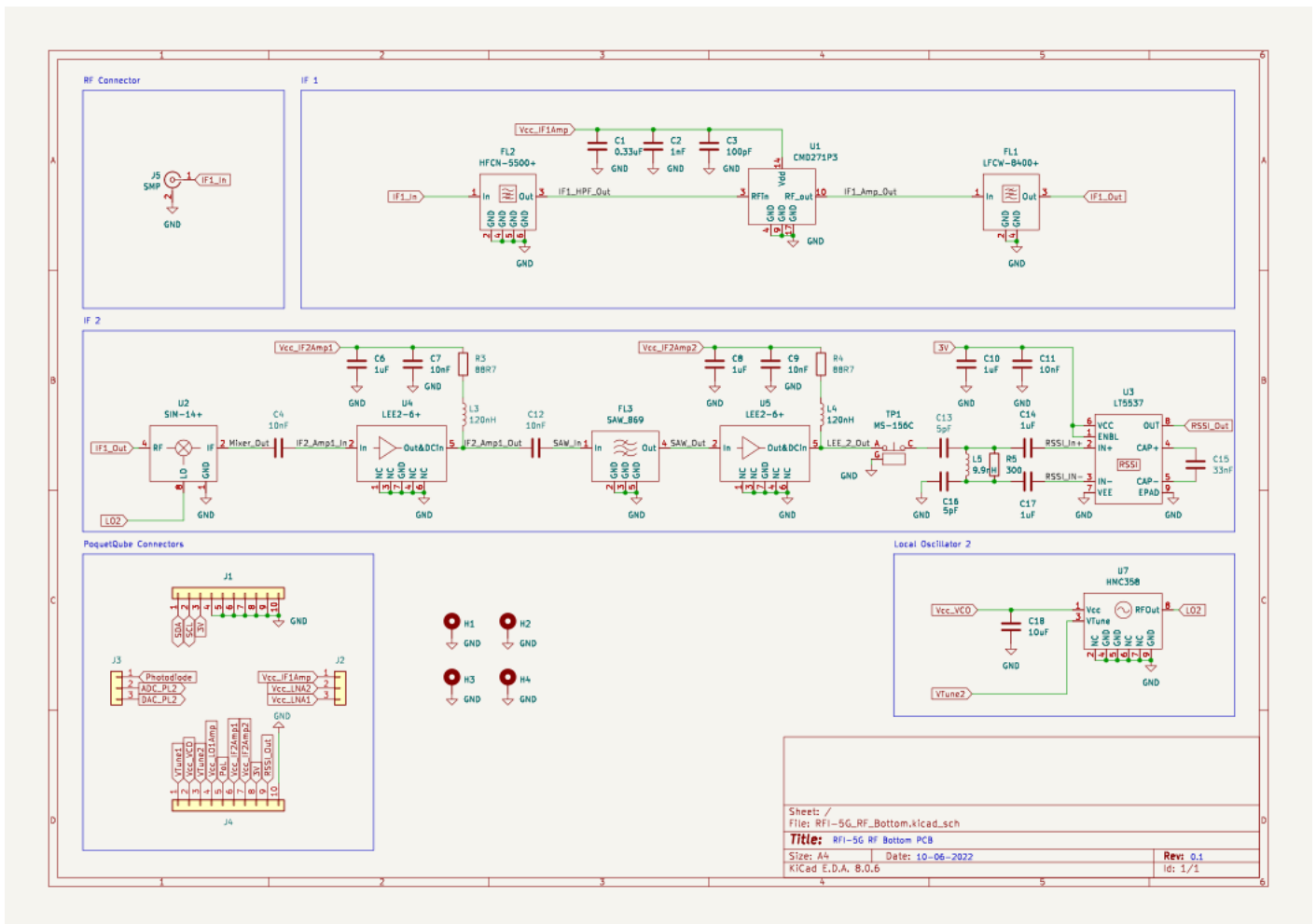
5. Additional Bandpass Filtering (SAW Filter)

- After amplification, the signal goes through FL3 (SAW-669), a SAW (Surface Acoustic Wave) filter with a specified center frequency of 669 MHz. SAW filters are known for their sharp frequency selectivity, providing excellent filtering to eliminate any residual high-frequency components and undesired harmonics.
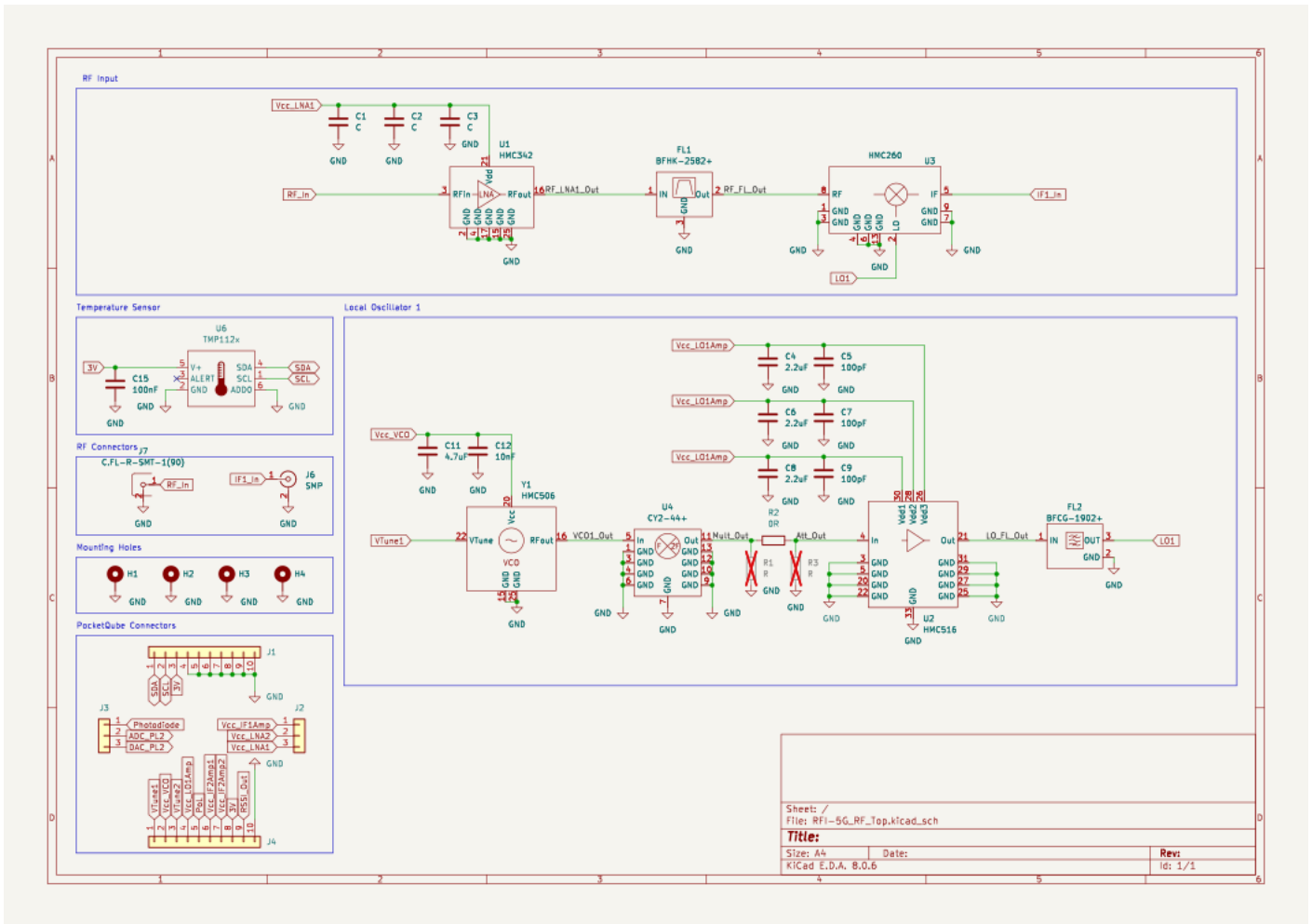
- The filtered signal is output as SAW_Out, which represents a clean, downconverted version of the original IF signal, now at a much lower frequency range, making it easier to handle and digitize in the later stages.

6. RSSI Measurement

- After downconversion, the signal is routed to the RSSI (Received Signal Strength Indicator) section, represented by U3 (LT5537). This IC provides an RSSI output, which gives a DC voltage proportional to the signal strength of the downconverted IF signal.
- The RSSI output is labeled RSSI_Out and is directed to the DAC input of the interface board, which apmplifies this signal and then sends it to the microcontroller in the satellite, allowing real-time monitoring of the received signal strength.
- Capacitors C14 (5 pF), C15 (33 nF), C16 (1 µF), and C17 (1 µF) in the RSSI section provide filtering and stabilization for the RSSI output, ensuring a clean and COHERENT signal for the DAC to measure.

7.3. Top PCB

8. PCBs

This payload is structured in 4 main block as stated in the *Payload block diagram* page. We will start by explaining the Interface PCB.

8.1. Interface PCB

This board is charge of electrically connecting the payload to the rest of the satellite, redistributing the grounding and converting it to a Multiple Point Ground (MPG), more specifically into two points, a single pin on the bottom and a multiple consecutive pin array on the top.

8.2. Bottom PCB

This board takes the IF signal from the Top PCB and downconverts it to be captured by the RSSI and output a voltage proportional to the signal power.

8.3. Top PCB

This board takes the signal from the antenna at the K Band and downconverts it to a Intermediate Frequency (IF).

Antenna Design

9. INTRODUCTION

The goal of PoCat payload 3 is to identify Radio Frequency Interference (RFI) in the lower Ka-band (24-25 GHz). A patch antenna is chosen as the resonant element for its lightweight, 2D design, and reduced size due to the inverse frequency-wavelength relationship. A basic Microstrip Patch antenna consists of a conductive patch on one side of a dielectric substrate, with a ground plane on the other, emitting radiation through fringing fields at the patch edge.

Requirements and specifications

Frequency operating range	Polarization	Dimensions	Input impedance
24-25 GHz	Lineal	40x40 mm^2	50 Ω

The design process is split in two main tasks. First, the single element design, includes choosing the appropriate substrate material, determine the patch antenna dimensions and the feedline that will match the patch with the rest of the array, and secondly, the design of the feeding network and the patches' distribution.

10. SINGLE ELEMENT: MICROSTRIP PATCH ANTENNA

SUBSTRATE

To optimize antenna performance, the choice of substrate is crucial. A low dielectric constant (ϵr) is preferred for minimal losses, improved efficiency, broader bandwidth, and better radiation. Increasing substrate height or reducing permittivity can also increase the bandwidth, but it may introduce undesired radiation and coupling to other components due to surface waves in the substrate. The loss tangent (tan(δ) or Df) is another main parameter affecting losses, with higher values indicating more dielectric absorption and losses. Rogers-5880, with a Df value of 0.0009 at 10GHz, is a suitable choice due to its low loss characteristics.
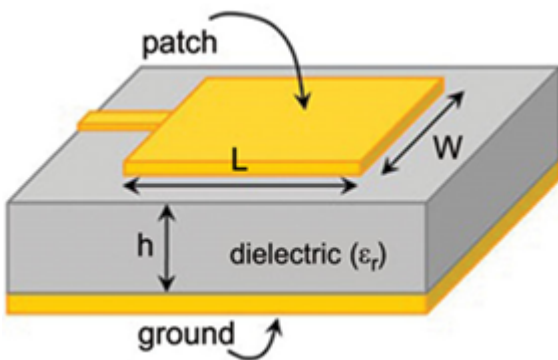
SINGLE ELEMENT DIMENSIONS

The initial patch dimensions are given by the following equation, which gives a patch side of ~4 mm using the Rogers-5880 substrate at a 24.5 GHz frequency.

$$f \approx \frac{c}{2L\sqrt{\varepsilon_r}} = \frac{1}{2L\sqrt{\varepsilon_0 \varepsilon_r \mu_0}}$$
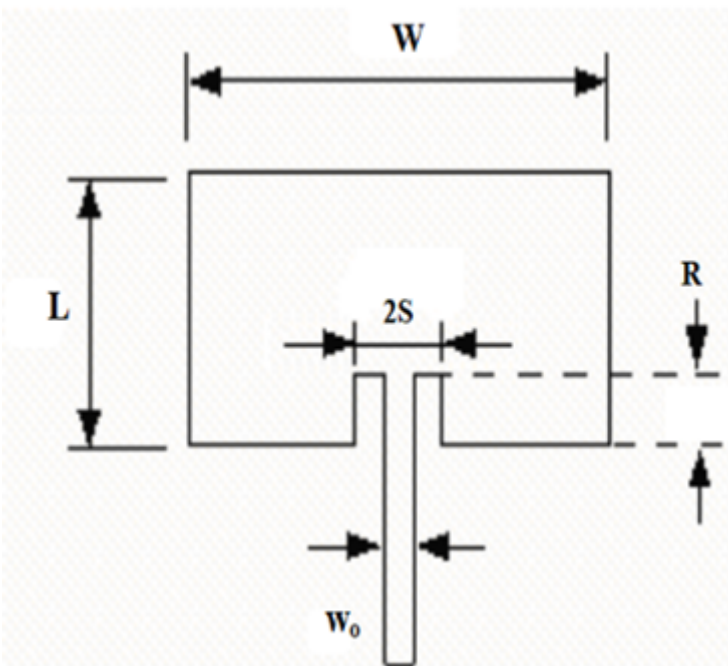
The length of the patches may be changed to shift the resonances of the centre fundamental frequency of the individual patch elements. The resonant input resistance of a single patch can be decreased by increasing the width of the patch. This is acceptable if the relation between the patch width and patch length (W/L) does not exceed 2 since the aperture efficiency of a single patch begins to drop, as W/L increases beyond this value.

Patch antenna main parameters:

PATCH ANTENNA MATCHING

In this project, the chosen method is to use a microstrip line attached at the edge of the patch, combined with adding an inset into the patch itself as shown in the following figure.

The longitude of the inset R can be calculated with the following equation where Zin(R) is the matching impedance and Zin(0) is the impedance at the edge of the patch (if the patch was fed in the end).
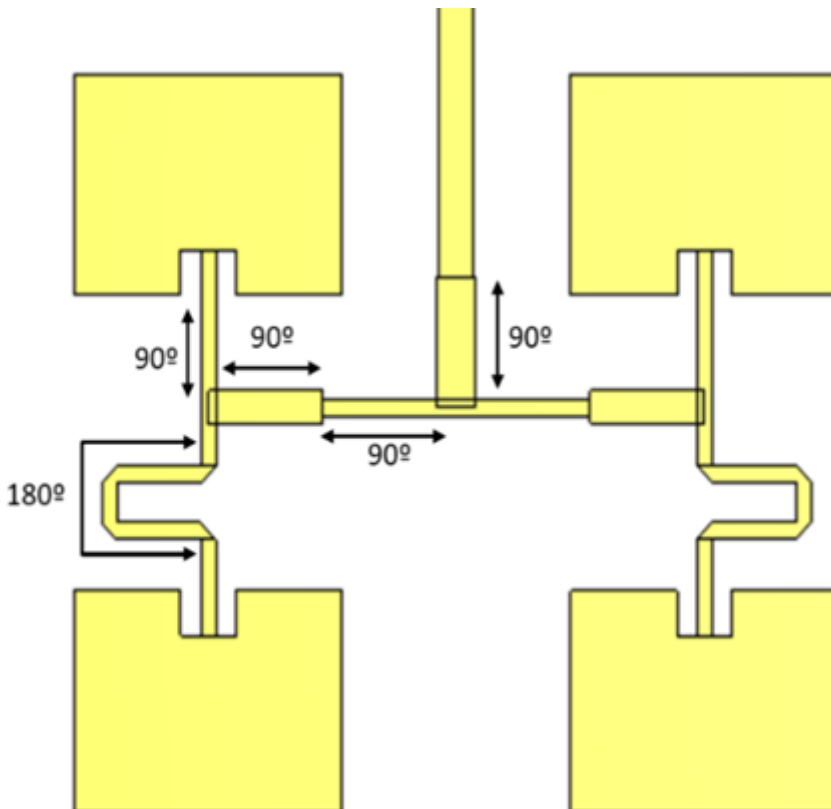
$$Z_{in}(R) = \cos^4\left(\frac{\pi R}{L}\right) Z_{in}(0)$$

Hence, by feeding the patch antenna as shown, the input impedance can be decreased to tune it at the desired value. The spacing S is a more challenging parameter to estimate, and it requires the simulation software to define it.

11. 2X2 PATCH ANTENNA ARRAY

The last step in the design process of a 2x2 patch antenna is to design the entire feeding network and the patches distribution. Knowing this field has been exhaustively studied, some made designs were considered at the beginning of this project, and researching about this technology, a design of a 24 GHz lineally polarized patch antenna, with the inset impedance matching technique, was found in an online repository from Zhengyu Peng, Ph.D. (Texas Tech University). In this manner, a reverse engineering study has been carried out to understand this design and then adapt it further to our requirements.

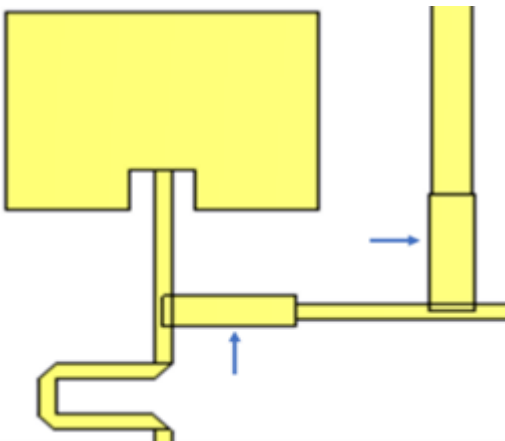Array model and electrical lengths of the feeding network:

By adding an extra 180º length to access the patches from the bottom of the structure, the waves from the two resonant elements are adding up to each other. In addition, the corner mitering technique has been used as well.

Mitred bend:

A 90º bend in a transmission line adds a small amount of capacitance to the transmission line, which causes a mismatch. A mitred bend as shown in the previous figure reduces some of that capacitance, restoring the line back to its original characteristic impedance. On the other hand, the whole structure impedance matching is done by two quarter-wave impedance transformers, adjusting the trace's width to obtain the desired characteristic impedance that sets 50 Ω at the output of the network.
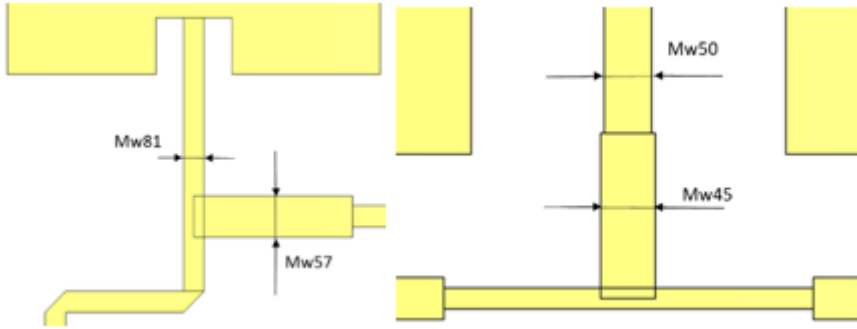
λ/4 impedance transformers:

The λ/4 impedance transformer design equation is included below, where Z0 is the characteristic impedance of the line, Zin the input impedance and ZL the impedance of the load.

$$\frac{Z_{in}}{Z_0} = \frac{Z_0}{Z_L}$$

Each line has been designed to match this equation according to the required input and output impedance:
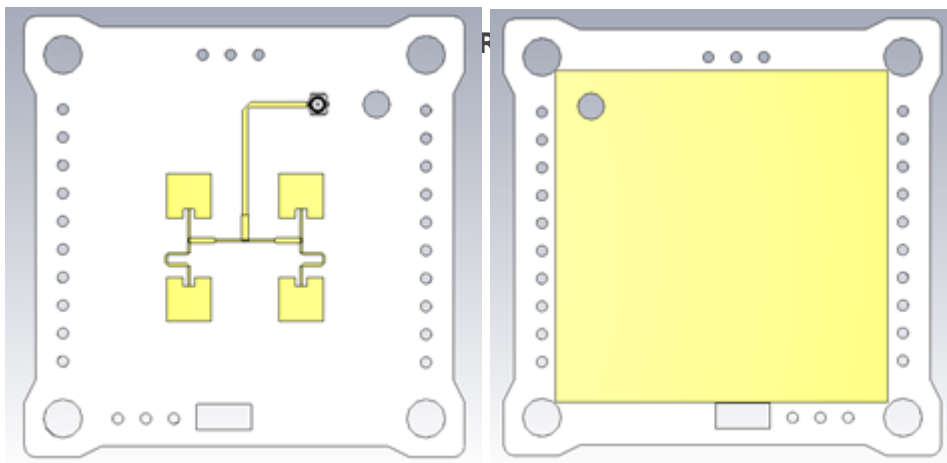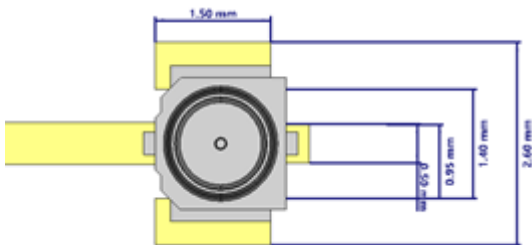
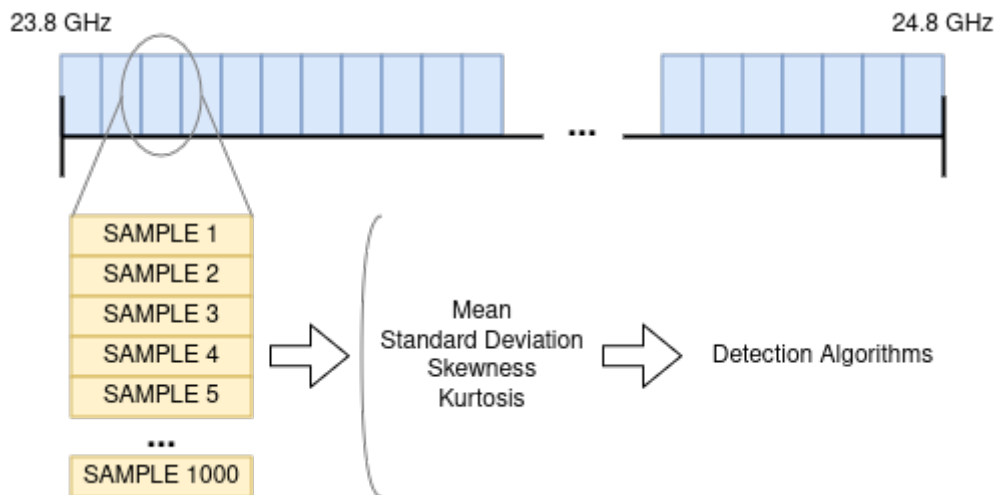- Mw45: 45 (Ω)
- Mw50: 50 (Ω)
- Mw57: 57 (Ω)
- Mw81: 81 (Ω)

CONNECTOR

The antenna will be positioned on the upper side of the satellite. Therefore, the dimensions of the substrate layer are determined by the PoCat's own dimensions, which measure 40x40 mm². To enable the assembly of the entire structure, the payload's board includes holes for pins and screws. Additionally, a HIROSE C.FL connector is attached to the top section of the structure, where it connects to the 50 Ω feeding line. This allows easy access for the coaxial cable to connect to the upper layer from below, requiring the incorporation of a hole into the substrate and ground plane, placed at the farthest point compatible with elements from payload 2.

Connector mounting pattern following HIROSE's recommendation:

Data Acquisition

12. Parameters:

```
struct rfi5gParameters{
  char* name;
  uint32_t timestamp;
  uint32_t temperature;
  uint32_t startFrequency;
}
```

13. Constants

13.1. General Constants

```
#define N_SAMPLES 1000
#define NUM_FREQ 62
#define R 10
```

N_SAMPLES: Number of samples to capture in one frequency bin.

NUM_FREQ: Number of frequency bins.

R: Number of repetitions for the calibration step.

13.2. Statistical Constants

```
#define KU_UPPER_THRES 3.3
#define KU_LOWER_THRES 2.7
#define SK_UPPER_THRES 200
#define SK_LOWER_THRES -200
```

Upper and lower thresholds for kurtosis and skewness.

Notice that skewness is multiplied by 1000.

13.3. Time Domain Constants

For the time domain the threshold is defined as $th = \beta\sigma + m$

```
#define AGGRESSIVENESS_TIME 1.5
#define PERCENTAGE_TH 0.01
#define K 1.3339
```

AGGRESSIVENESS_TIME: Aggressiveness Time (aka β) is an empirical value obtained by simulating different INR values.

PERCENTAGE_TH: Percentage Threshold is the minimum percentage to consider the existence of an interferent signal, it is defined as the minimum number of detection out of N_SAMPLES.

13.4. Frequency Domain Constants

```
#define AGGRESSIVENESS_FREQ 1.5
```

AGGRESSIVENESS_FREQ: Aggressiveness Frequency is an empirical value obtained by simulating different INR values.

14. Structures Definition

```
typedef struct{
    uint16_t mean;
    uint16_t stdv;
    uint16_t ku;
    int16_t sk;
    uint16_t Ndet;
    uint8_t decision;
} tRFIbinCapture;
```

mean: Mean is a statistical parameter that shows the central tendency of the distribution.

stdv: Standard Deviation is the square root of the second standardized moment, it measures the dispersion of the distribution.

sk: Skewness, also known as the third standardized moment, is a metric that characterizes the asymmetry of the distribution.

ku: Kurtosis is the fourth standardized moment, that measures how big are the tails of the distribution.

Ndet: Number of detections counts the number of samples that had surpassed the threshold in time domain algorithm.

decision: Decision is an 8 bits variable, which flags with a pair of bits if an alogorithm has detected an interference.

From the least significant bit to the more significant bit, the flags are grouped in pairs:

-The first two bits are turned on if the statistical domain algorithm detects an interference.

-The second pair of bits are activated if the time domain algorithm detects an interference.

-The third pair of bits are activated if the frequency domain algorithm detects an interference.

-The fourth couple of bits is the combination of the previous decisions, if any algorithm has detected an interference these two bits are turned on.

Due to the possibility of ions or electromagnetic radiation to strike into the electronic circuits, causing an unwanted bit change, commonly refered as single event upset (SEU), each decision bit has a redundancy of one.

```
typedef struct{
    uint16_t id;
    tRFIbinCapture captures[NUM_FREQ];
} tRFIsweepCapture;
```

tRFIsweepCapture: This struct consists in the frequency axis data, since the system does not do a continuous frequency sweep, the axis is discretitzed in NUM_FREQ bins.

id: It is the identifier of a capture.

15. Comms considerations

> As of now this section is in development

Non mandatory data:

- Frequency bins with 0 Number of Detections.
- Statistical parameters
- sweepCapture.Id (it is already identifies by timestamp)
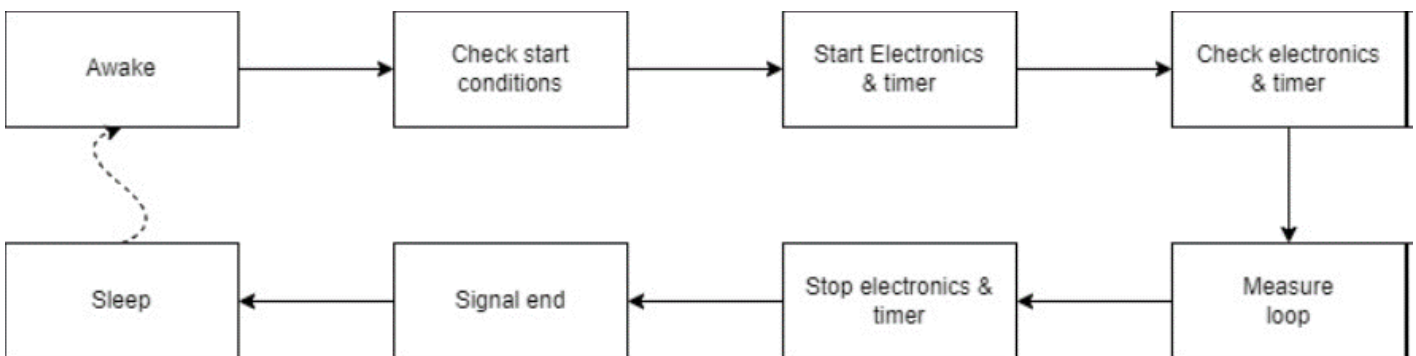
RFI-Dedicated Thread

16. RFI Thread

16.1. Introduction

Like many other subsystems, the Payload is a self-contained sub-system and so it has its own FreeRTOS Thread. This thread is concieved to be able to control each of the two RFI monitoring payloads.
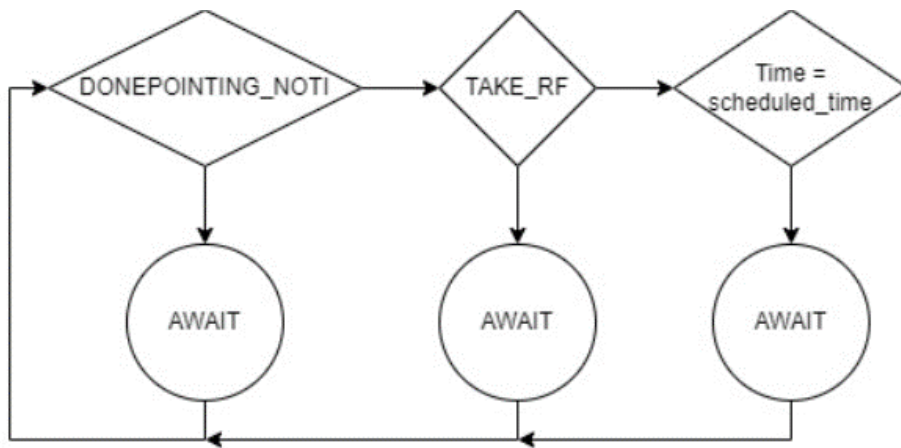
As an overview, the thread is structured as secuential general operations. And each of them is a key step in the process of making the payload work.

16.2. Block Diagram

To begin, the general behavior of the code is defined, since it is basic to have it structured from the most generic functions to the most specific ones. This general structure is basic since it is the one that will be in direct "contact" with the OBC code, and its structure and functioning requirements.
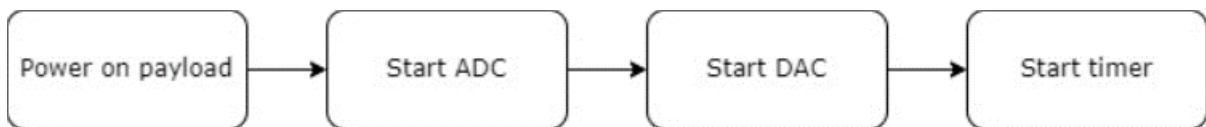

This figure, as stated above, defines how the payload code is structured and its sequential steps. Note that the discontinuous arrow indicates that once the loop has finished, the payload thread enters a sleep mode, waiting for the OBC to awaken him again to restart the loop. So, the first to take a deeper look into is going to be the Check start conditions block:
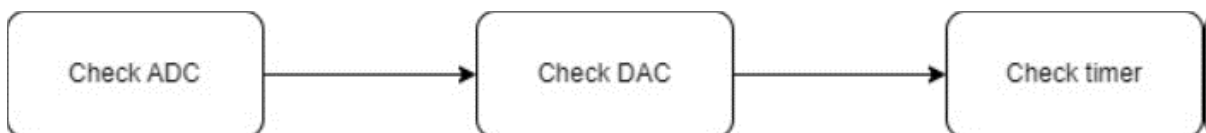
As it can be seen above, the first thing to do in order to get the payload running properly is to check if the conditions required by the Ground Station user are met, this includes three things:

1. The satellite is pointing at the desired region of the Earth steadily.
2. The order to make an RFI measurement has been truly received.
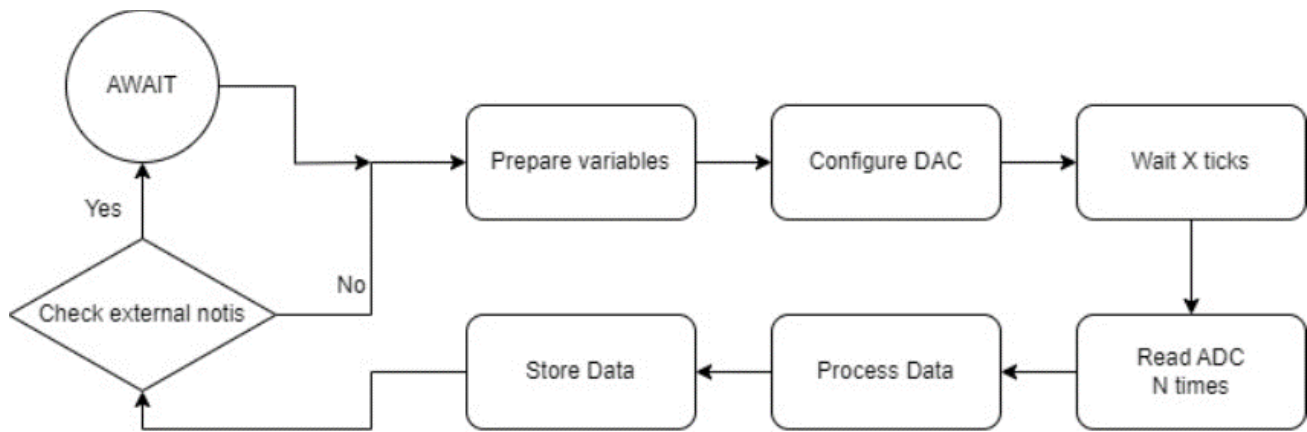3. It is the scheduled moment to take the photo.

If none of these requirements are met, the thread awaits until it is signaled by the OBC and then rechecking everything again. Once the check has been succeed, it is time to Start the electronics and the timer:

Obviously, the first step is to power on the payload and consequently all its elements. Then the ADC and DAC are initialized and started. The same happens to the timer. Once they have been started it is time to make sure that they work as expected:

Now the ADC and DAC are checked and calibrated, the timer is only checked. This is done to assure that when using them in the measurements they don't give false reading due to a malfunction. Having everything powered on, initialized and checked, the measure loop can begin:

This loop is run as many times as needed in order to scan all the frequency bins forming the L or Ka bands. This scans are slow, so not to block the whole satellite system, every time a frequency bin is scanned the thread checks for notifications coming from the rest of the PQ to pause itself if necessary. Then, once the satellite does not need to have the RFI thread stop anymore, the RFI thread continues from where it was.

In order to bring the explanation to a lower level, the list below explains each block step by step:

- Prepare variables: Every variable that is going to be used during the measure loop execution needs to be initialized to ensure a solid structure in the RAM (Random Access Memory).
- Configure DAC: As explained in Chapter 4.2.3, the DAC (Digital to Analog Converter) is configured to make the oscillator output a certain frequency (depending on the frequency bin that wants to be analyzed) by inputting the accordingly calculated voltage.
- Wait X ticks: a yet to be calculated amount of clock ticks is waited to ensure that the frequency from the CO (Controlled Oscillator) is stable.
  - The amount of ticks needed depends on the clock speed, and DAC configuration and stabilisation time, which can be found in the microcontroller datasheet. The amount of ticks awaited must exceed an equivalent time of 7.5us.
  - This calculation is done taking into account the clock speed and therefore the tick period. This results in the next formula: $X = 7.5/f_{clk}[MHz]$
- Read ADC N times: The ADC reads the voltage from the RSSI output and converts it to a digital value. This is done N times for the posterior time domain analysis of the samples. The value of N is calculated by dividing the BW (Bandwidth) of the band with the RSSI BW, resulting in the next formula: $N = BW/BW_{RSSI}$.
  - For the L band: Since the RSSI BW is 4 MHZ, the resulting $N = 250$.
  - For the Ka band: Since the RSSI BW is 16 MHZ, the resulting $N = 63$.
- Process Data: With the raw ADC (Analog to Digital Converter) values, calculate different statistical parameters to represent that frequency bin. Those will be stored, whereas the raw values will not.
- Store Data: Store the data mentioned before in a array that will store the statistical data from each frequency bin.

Now that the measurements have been done, it is time to power off this subsystem:

So, first both ADC and DAC are stopped, then the payload is powered off and then the timer is stopped.
To finish the thread execution, the end of the payload work is signaled to the OBC and then the thread enters sleep mode.

17. Detection algorithms

17.1. Temporal algorithm

The aim of this sub-algorithm is to detect pulses through Envelope Detection, a straightforward technique used for RFI monitoring. It involves sampling the input signal and comparing its power with a predetermined threshold. The detector continuously observes the power of the received signal in each temporal sample and establishes a threshold based on the typical noise floor level. When the power level of the samples exceeds this threshold, the detector interprets it as a presence of RFI.

Although the Envelope Detection algorithm has been chosen, other time domain detection algorithms exist such as the FFT (Fast Fourier Transform) based ones. FFT is the most important calculation when talking about time sampled signal processing because it allows to not only analyse the signal in the temporal domain but also in the frequency one. And by combining these two ones, advanced algorithms can be elaborated.

In addition to that, despite the very limited processing capabilities of the microcontroller used in the satellite, some advances are being done. Some preliminar tests have already proven the possibility to compute FFTs in that microcontroller. In the following weeks the integration of those algorithms with the rest of the code will be tried and tested.

Now the mathematical algorithm will be explained. First, the temporal samples vector, expressed as: $x[n]$;being N the number of samples taken Is iterated in order to calculate its mean:

$$\overline{x} = \frac{1}{N} \cdot \sum_{i=1}^{N} x_i$$

Finally, if the $\overline{x}$ is higher or lower than an arbitrary threshold the decision of whether there is in fact a signal or not is taken. This threshold is the most important part of the algorithm and its value highly affects the accuracy of the decision.

17.2. Statistical Algorithm

The purpose of this sub-algorithm is to estimate if there are signals based on their third and fourth statistical moments. These moments are extracted from the temporal samples taken in each frequency bin.

However, there are many other statistical parameters that can be taken into account, such as the standard deviation, the covariance or the correlation. Unlike the reason above, these parameters will not be used because they are not considered necessary with the given skewness and kurtosis reliability.

Now the kurtosis formula will be explained:

$$Ku = \frac{\frac{1}{N} \cdot \sum_{i=1}^{N}(x_i - \overline{x})^4}{\left(\frac{1}{N} \cdot \sum_{i=1}^{N}(x_i - \overline{x})^2\right)^2}$$

Where: x_i is the i-th sample.
In the numerator of the fraction there is the calculation of the fourth statistical moment, while in the denominator there is the standard deviation elevated to the fourth power. Now the skewness formula will be explained:

$$Ku = \frac{\frac{1}{N} \cdot \sum_{i=1}^{N}(x_i - \overline{x})^3}{\left(\frac{1}{N} \cdot \sum_{i=1}^{N}(x_i - \overline{x})^2\right)^{\frac{3}{2}}}$$

Where: x_i is the i-th sample.
In the numerator of the fraction there is the calculation of the third statistical moment, while in the denominator there is the standard deviation elevated to the third power.

Again, as explained in the time domain algorithm, the decision of the statistical algorithm is based on the comparison between the statistical parameters and predefined thresholds that, if exceeded or not, a decision is then made.

17.3. Frequency Algorithm

The aim of this sub-algorithm is to detect signals in the frequency domain and eventually mitigate them by frequency blanking. This technique operates in a similar manner to Envelope Detection, but in the frequency domain. If a significant increase in power is observed at a particular frequency bin compared to its neighbouring bins, it may indicate the presence of interference. These power peaks are more easily detected when they have high power in a narrow bandwidth.

This analysis is done by comparing the received power from adjacent frequencies and applying a threshold to distinguish these values. So, if the algorithm detects a signal that is above that threshold, it decides that it is in fact an Interference.